

Compal Confidential

V15 /DH5VF

V17 /DH7VF

Vx15/DH53F

Vx17/DH73F

MB Schematic Document

**Intel CoffeeLake H
Nvidia N17P-G0/G1**

LA-F951P

Rev:1A

2018.02.22

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	Cover Sheet
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size	Rev
				Custom	1.0
Date: Thursday, February 22, 2018				Sheet	1 of 67

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{BD} min	V _{BD} typ	V _{BD} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFF
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
VRAM BOM Select	X76@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
USB charger	CHG@
non USB charger	NCHG@
G-Sensor	GSEN@
Thermal sensor	TMS@
for SW debug board	UART@
Intel CNVi (reserve)	CNVI@
Finger Print	FP@
FingerPrint(with PBA)	PBA@
USB Type-C CC controller	TYPEC@
EMI/ESD requirement	EMC@
EMI/ESD require reserve	XEMC@
FP ESD requirement	FPEMC@
28P keyboard connector	V15@
32P keyboard connector	VX15@
SATA HDD W REDRIVER	SATARD@
SATA HDD WO REDRIVER	SATANRD@
NV N17P-G0(1050)	G0@
NV N17P-G1(1050TI)	G1@
i5 CPU	i5@
i7 CPU	i7@
ALC 255 Codec	255@
ALC 256 Codec	256@
Codec LDO mode	LDO@
Codec Switch mode	SWR@

State

SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	HIGH	HIGH	HIGH	ON	ON	ON	ON
RAM	LOW	HIGH	HIGH	ON	ON	OFF	OFF
Disk	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator.	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.9VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+1.8VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK (+3VS)	LIS3DHTR(G-sensor)	0x30		
	N17P-GX (VGA)	0x9E		
	EC			
	CC controller 179F			
	TMS			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 level BOM table

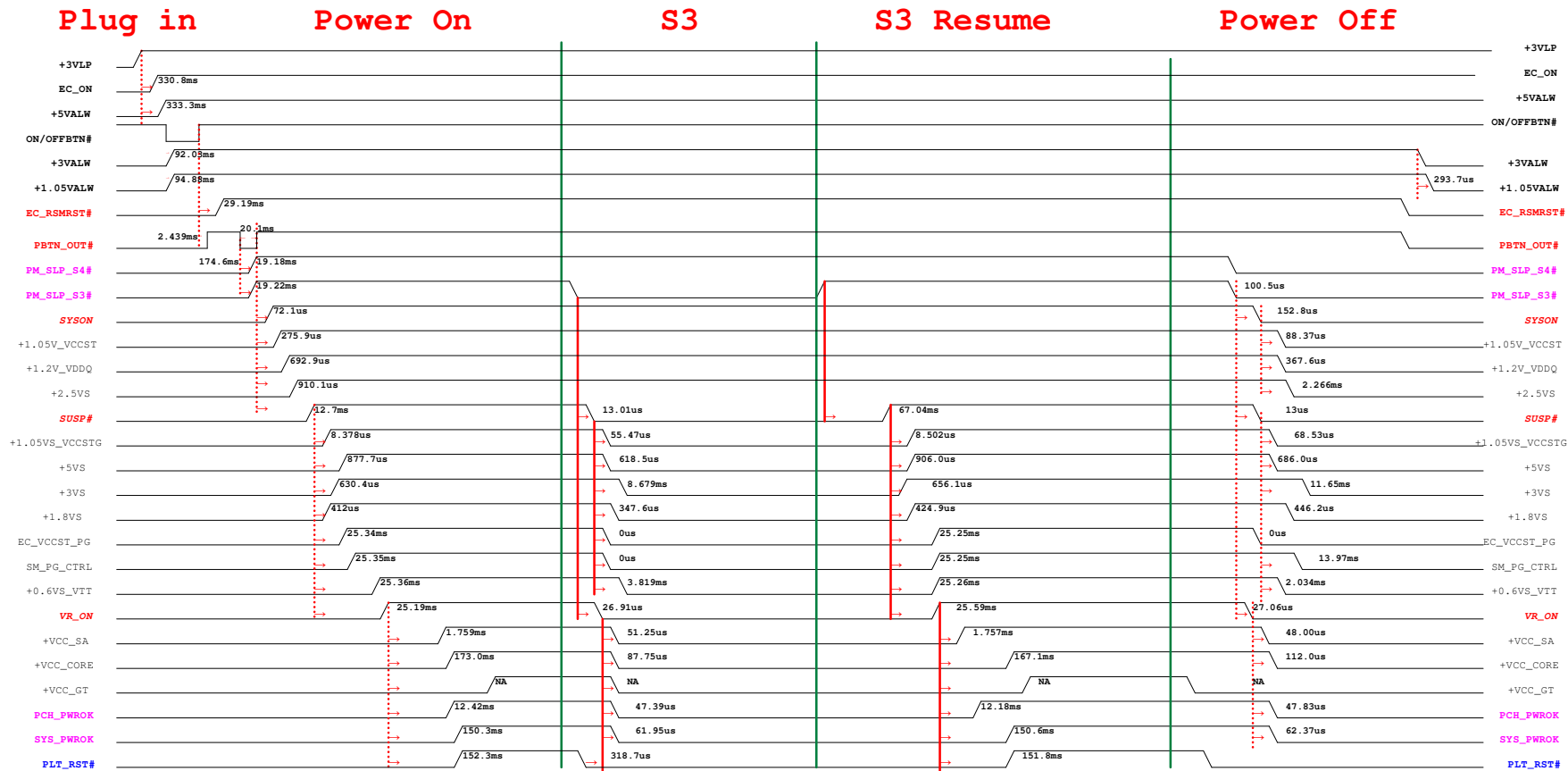
43 Level	Description	BOM Structure
Vx15, Sienta		
43IAB1B0L60	SMT MB AF951 DH53F I5QP89 PG1 4G 32HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/VX15@/SATANRD@
43IAB1B0L61	SMT MB AF951 DH53F I7QP86 PG1 4G 32HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/VX15@/SATANRD@
43IAB1B0L66	SMT MB AF951 DH53F I78750 PG1 4G 32HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/VX15@/SATANRD@
V15, Vx15-Fresd		
43IAB1B0L62	SMT MB AF951 DH53F I3QP89 PG0 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G0@/V15@/SATANRD@/FP@
43IAB1B0L63	SMT MB AF951 DH53F I78750 PG0 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G0@/V15@/SATANRD@/FP@
43IAB1B0L64	SMT MB AF951 DH53F I5QP89 PG1 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G1@/V15@/SATANRD@/FP@
43IAB1B0L65	SMT MB AF951 DH53F I78750 PG1 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATANRD@/FP@
V17		
43IAB1B0L65	SMT MB AF951 DH7VF I5QP89 PG0 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G0@/V15@/SATANRD@/FP@
43IAB1B0L65	SMT MB AF951 DH7VF I78750 PG0 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G0@/V15@/SATANRD@/FP@
43IAB1B0L65	SMT MB AF951 DH7VF I5QP89 PG1 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G1@/V15@/SATANRD@/FP@
43IAB1B0L65	SMT MB AF951 DH7VF I78750 PG1 4G 28HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATANRD@/FP@
VX17		
43IAB1B0L68	SMT MB AF951 DH7VF I5QP89 PG1 4G 32HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATANRD@/FP@
43IAB1B0L69	SMT MB AF951 DH7VF I78750 PG1 4G 32HDM1	255@/CHG@/CMC@/CNV1@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATANRD@/FP@

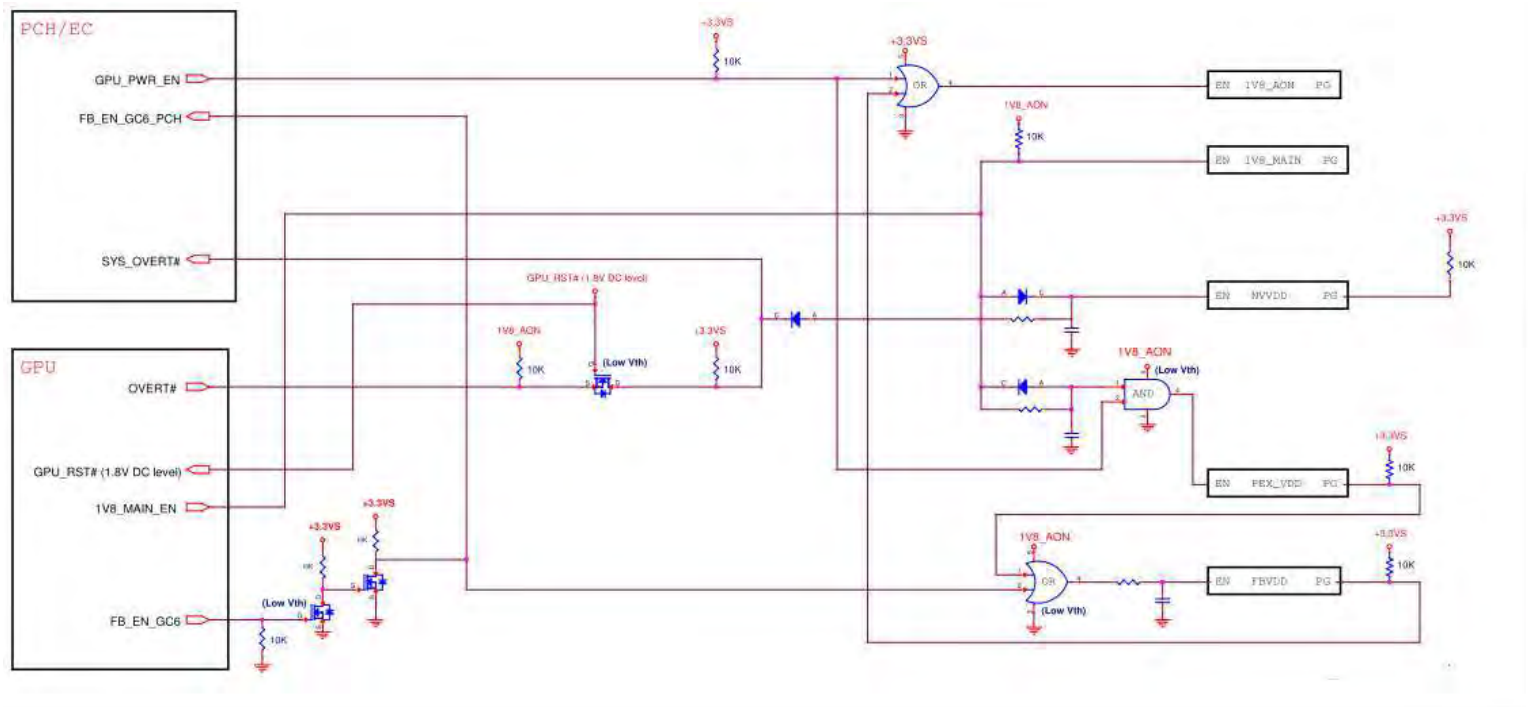
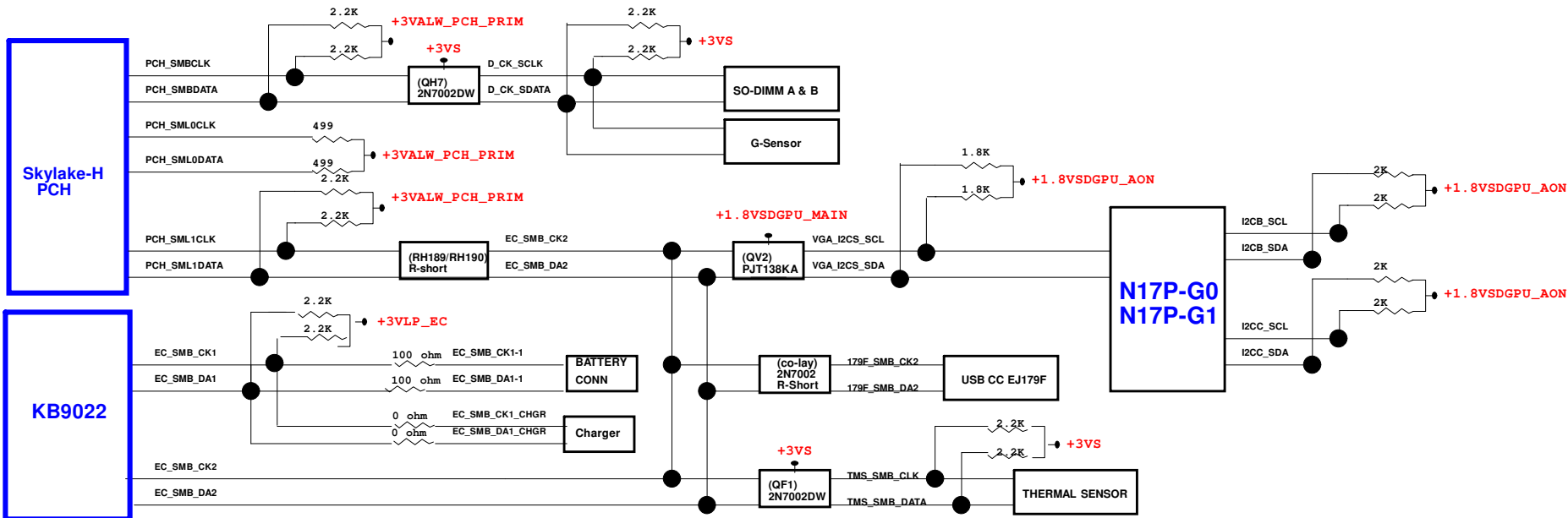
BOARD ID Table

V series		Vx series	
Board ID	PCB Revision	Board ID	PCB Revision
0	0.1	10	0.1
1	0.2	11	0.2
2	1.0	12	1.0
3	1.A	13	1.A
4		14	
5	1.0	15	1.0
6		16	
7		17	
8		18	
9		19	

X76730BOL51 SAMSUNG1280
X76730BOL52 HYNIX1280
X76730BOL53 SAMSUNG2560
X76730BOL54 HYNIX2560
X76730BOL55 MICRON2560

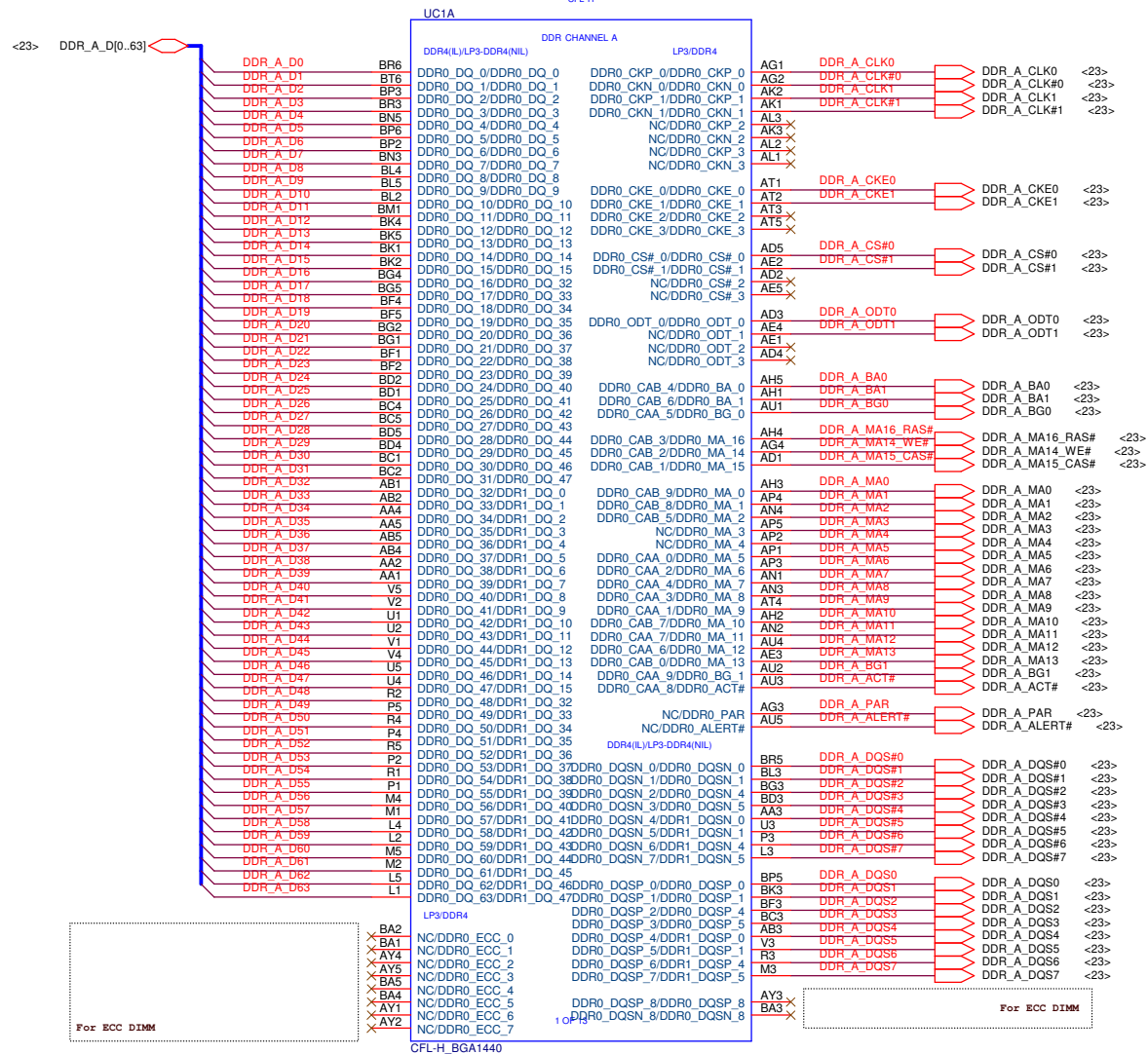
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Document Number
				DH5VF M/B LA-F591PR01
				Date
				Thursday, February 22, 2018
				Sheet 3 of 37

BIOS ver: V0.02W1
EC: ver: V002AT04



CHANNEL-A

Interleaved Memory

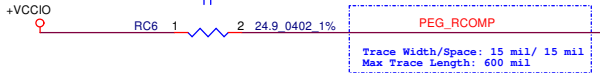


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	CFL-H(2/8)DIMMA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	DH5VF M/B LA-F591PR01
				Date:	Thursday, February 22, 2018
				Sheet	8 of 67
				Rev	1.0

PEG&DMI

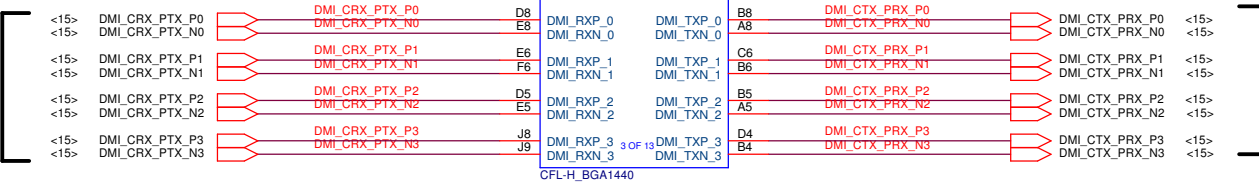
To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed



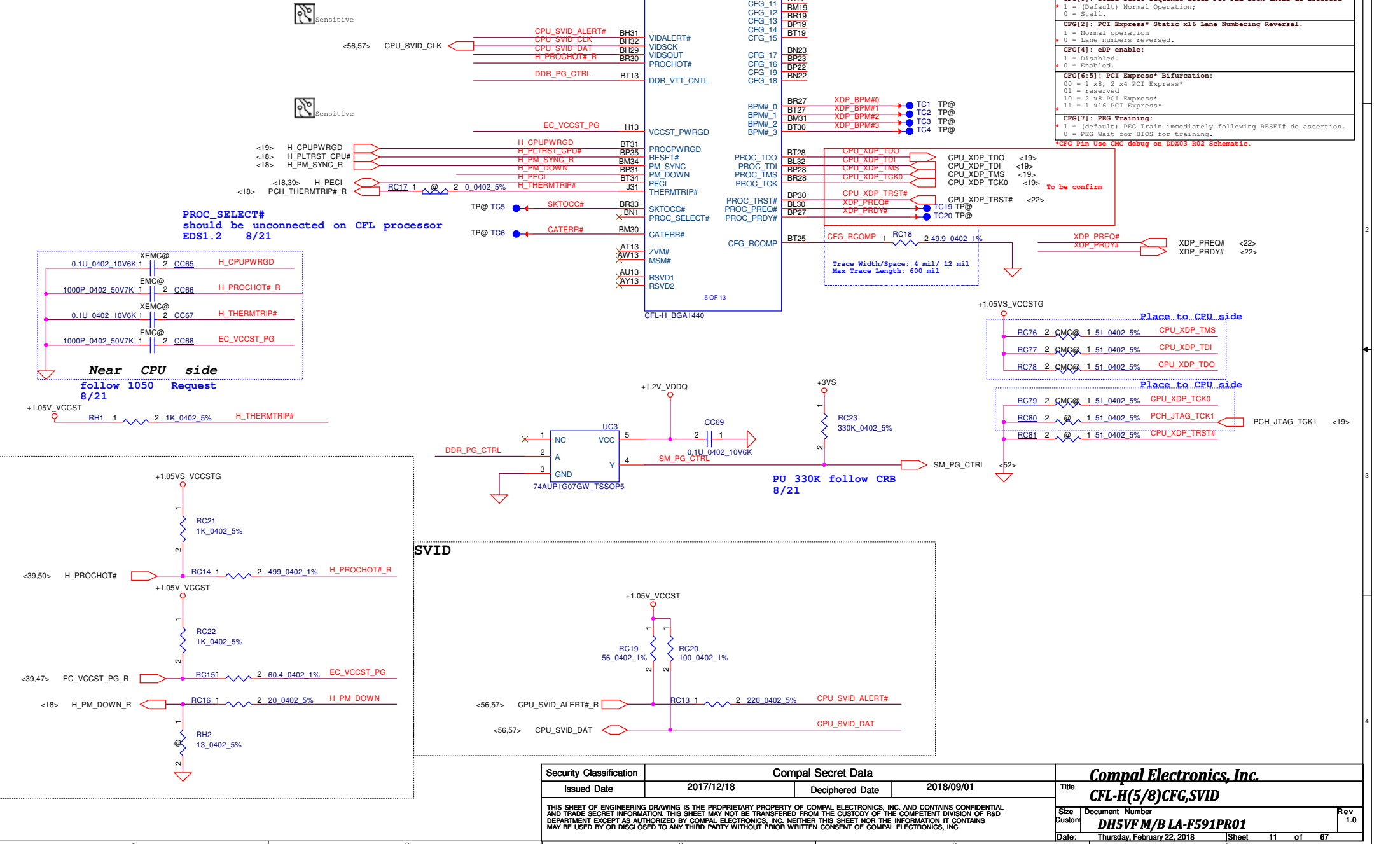
To PCH

To PCH



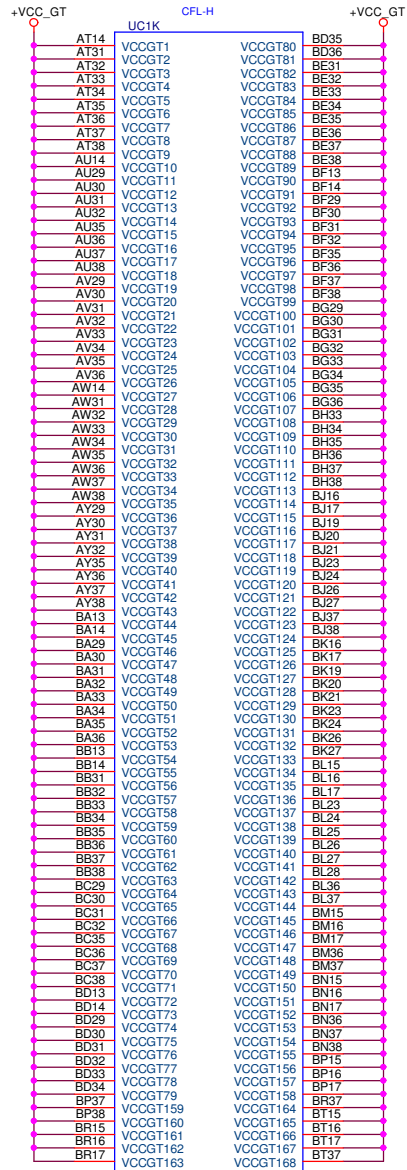
CFL-H_BGA1440

571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.



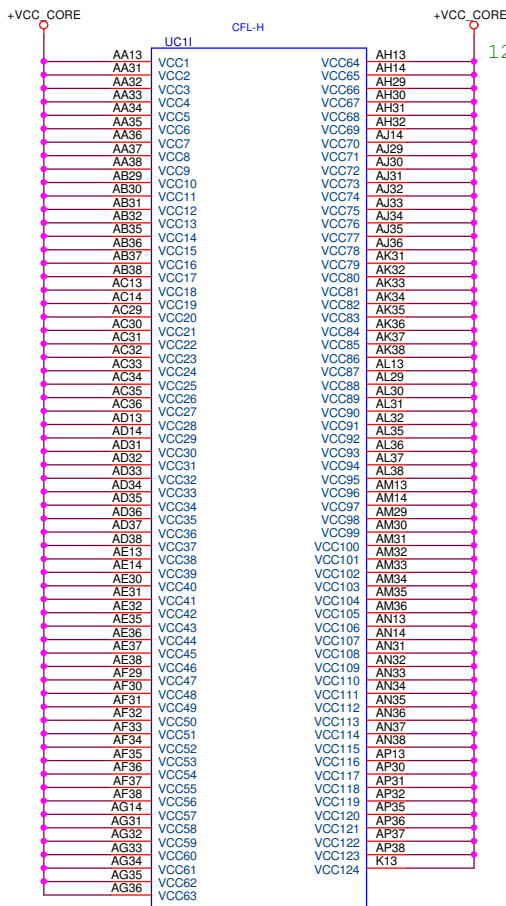
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2017/12/18				Title			
Deciphered Date				2018/09/01				CFL-H(5/8)CFG,SVID			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size				Document Number			
				DH5VF M/B LA-F591PR01				Rev			
Date:				Thursday, February 22, 2018				Sheet			
				11				of			
				67							

GT
32000mA (Hexa Core GT2)



CFL-H_BGA1440

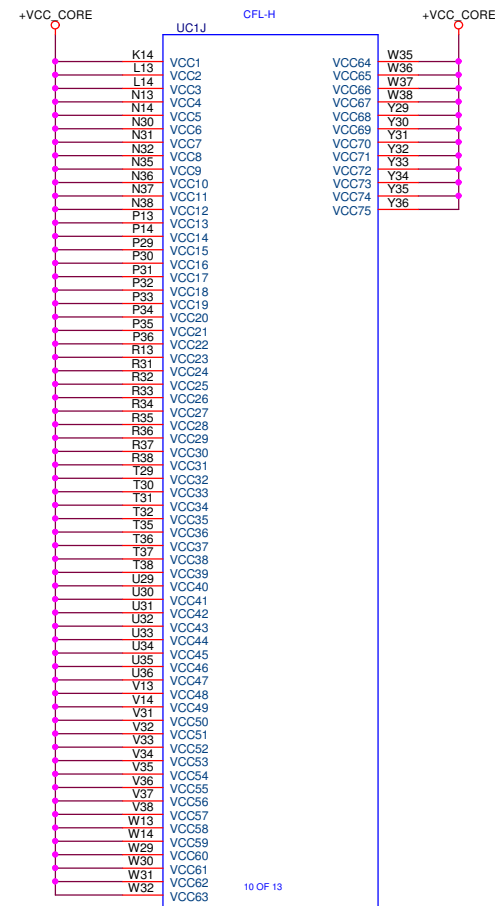
1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



CFL-H_BGA1440

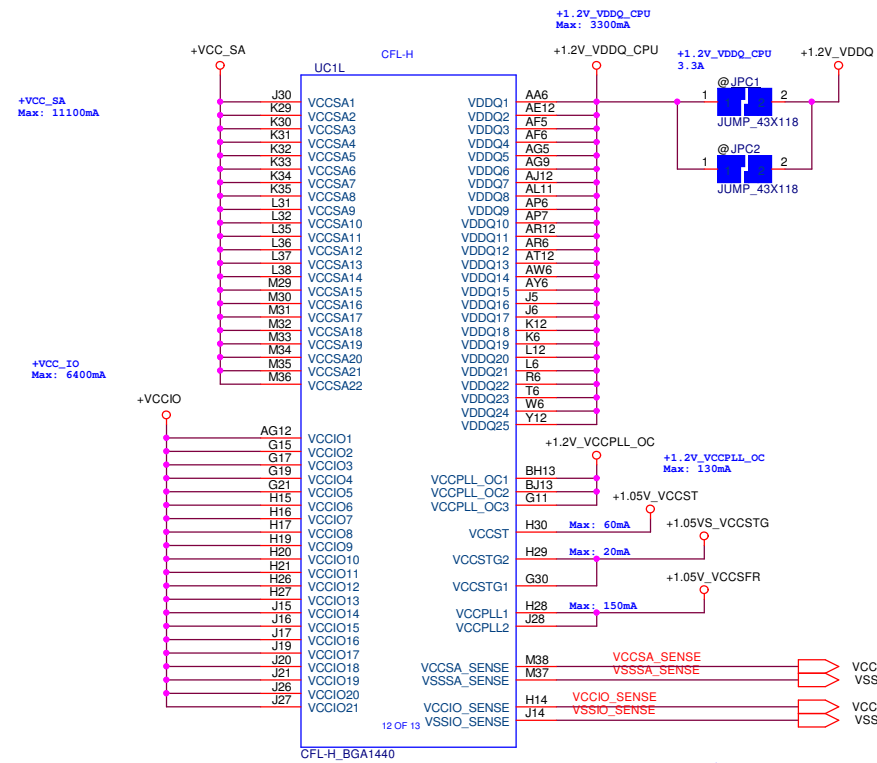
1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

128000mA (Hexa Core GT2)

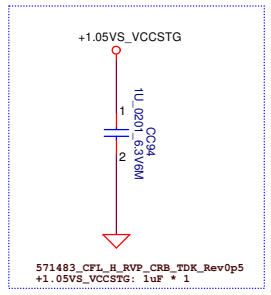
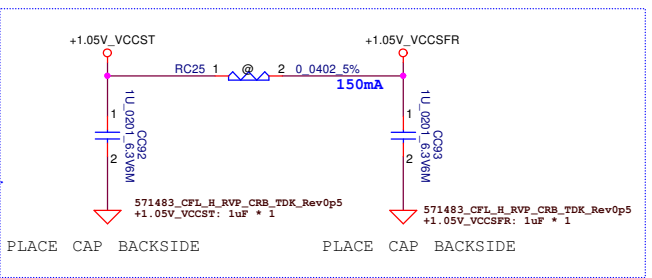
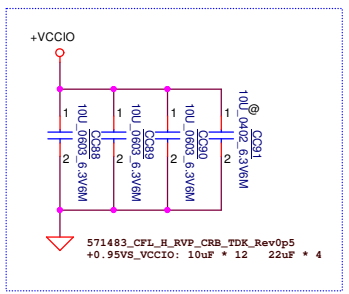
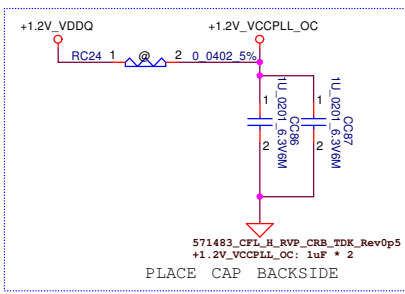
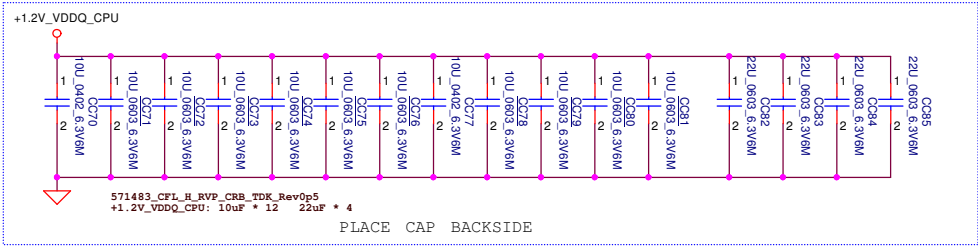


CFL-H_BGA1440

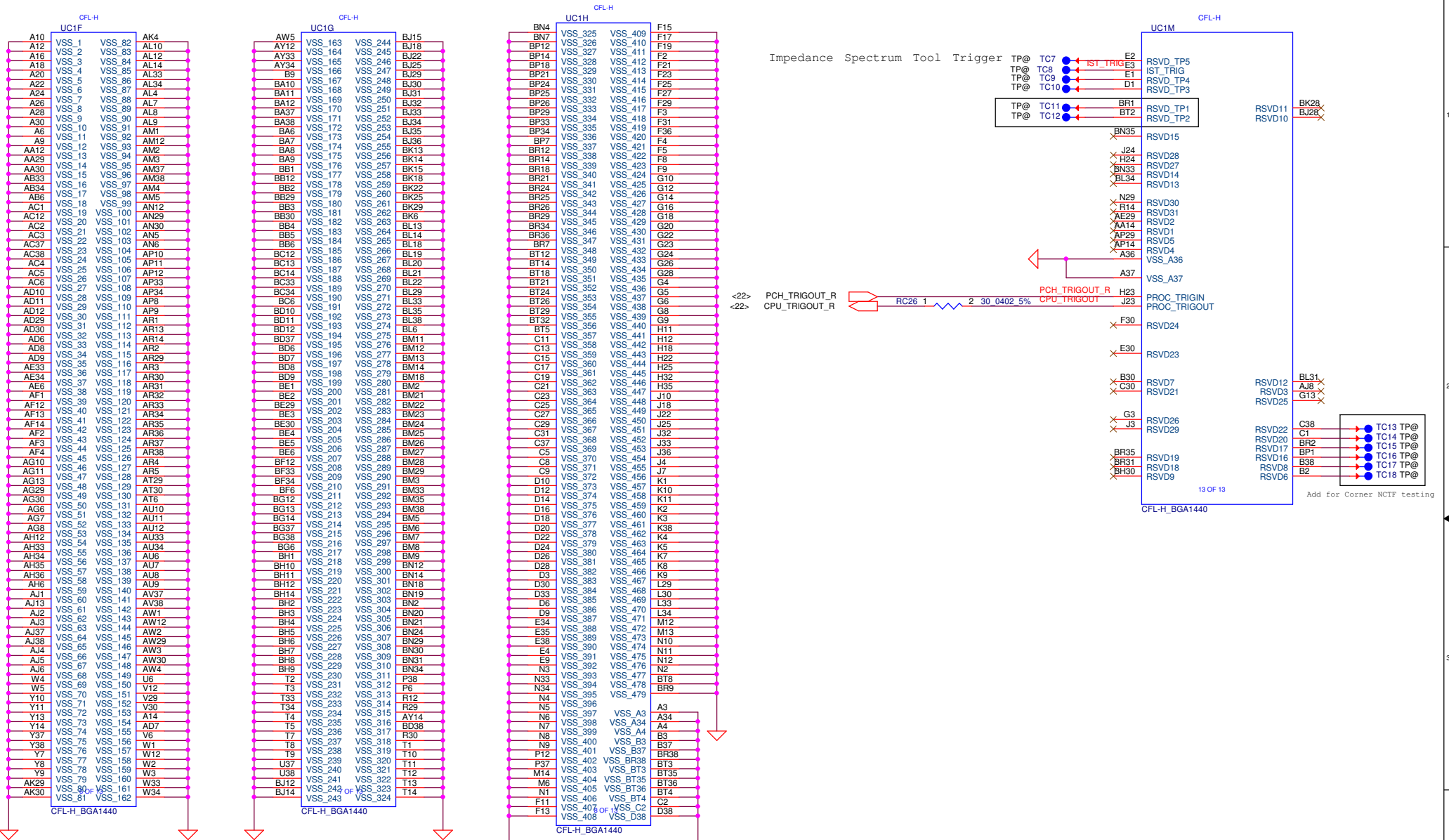
Security Classification		Compal Secret Data		Compal Electronics, Inc.							
Issued Date		2017/12/18		Deciphered Date		2018/09/01		Title		CFL-H(6/8)VCC CORE/GT	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Size	Document Number		Rev
								Custom	DH5VF M/B LA-F591PR01		1.0
								Date:	Thursday, February 22, 2018		Sheet

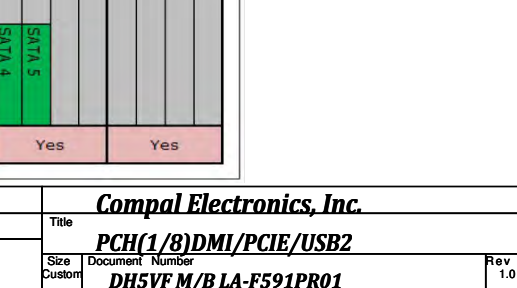
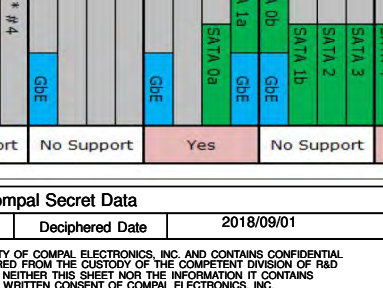
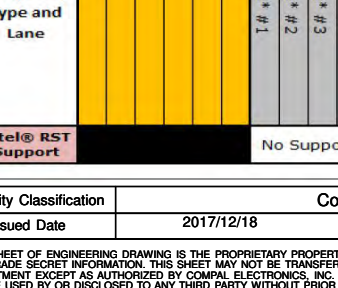
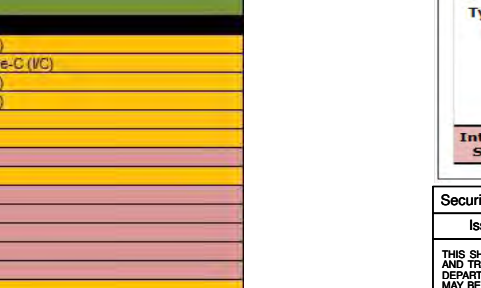
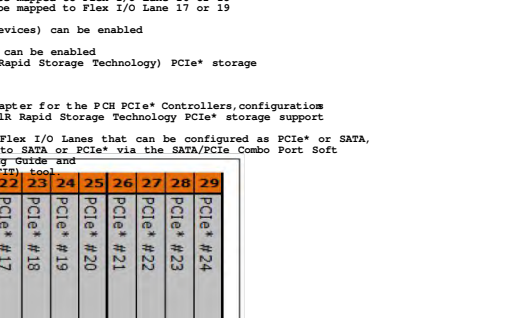
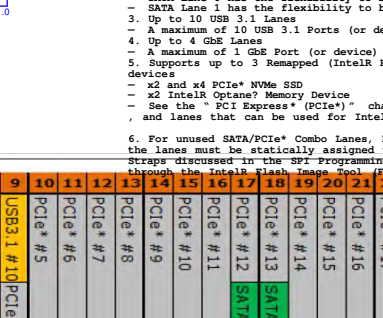
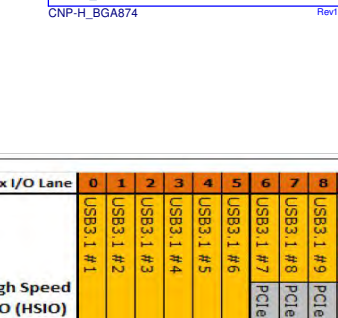
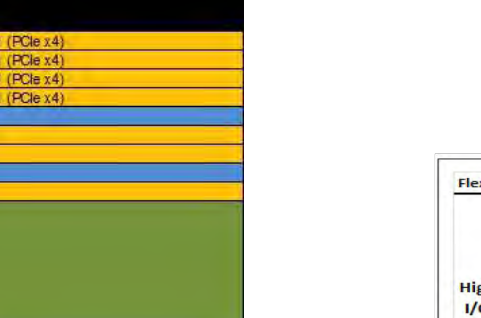
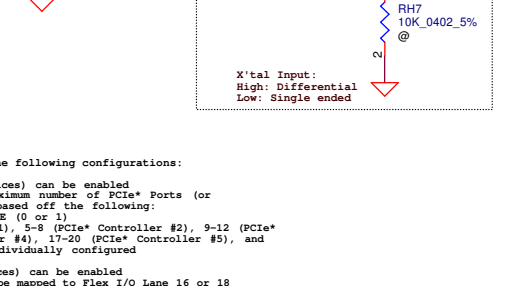
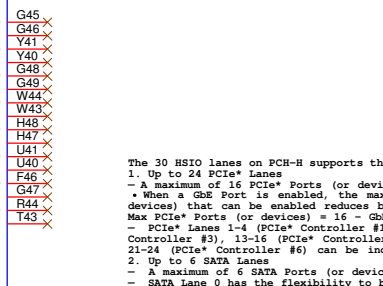
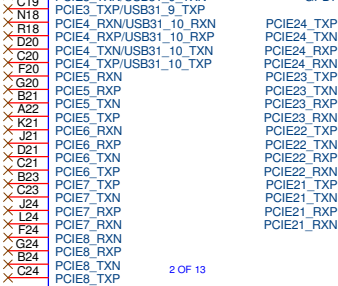
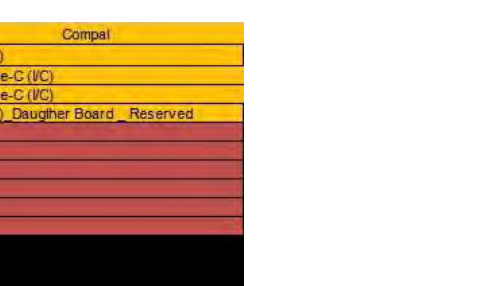
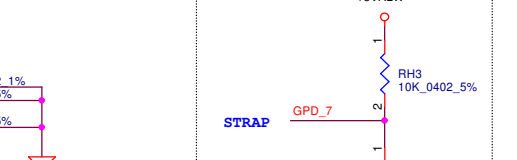
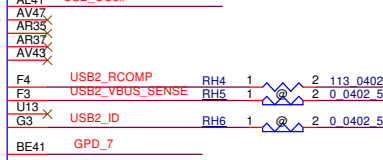
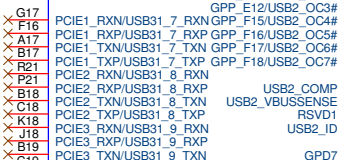
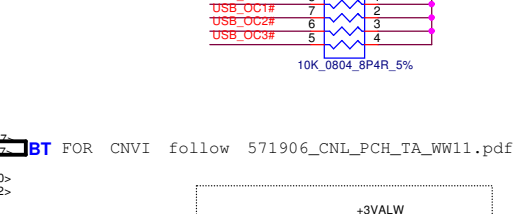
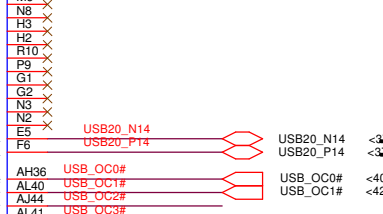
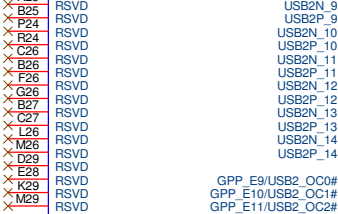
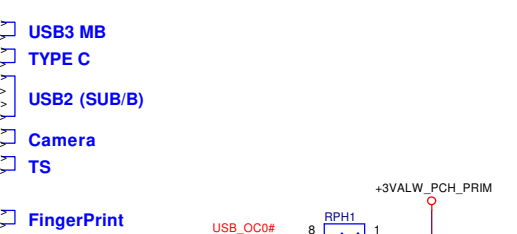
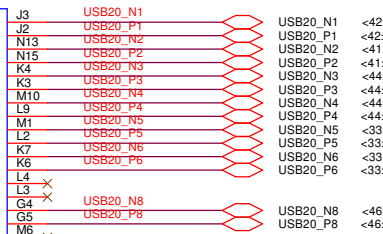
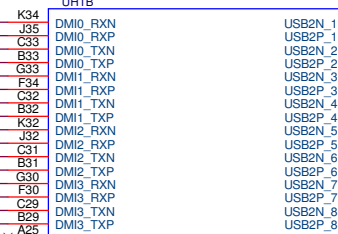
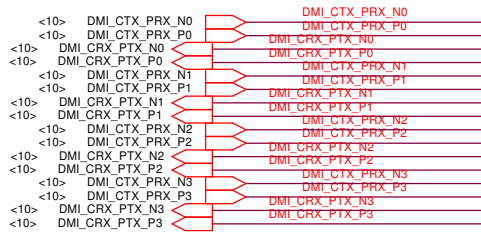


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	CFL-H(7/8)VCCSA/VCCIO/VDDQ
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				Date	Thursdays, February 22, 2018
				Sheet	13 of 67
				Rev	1.0



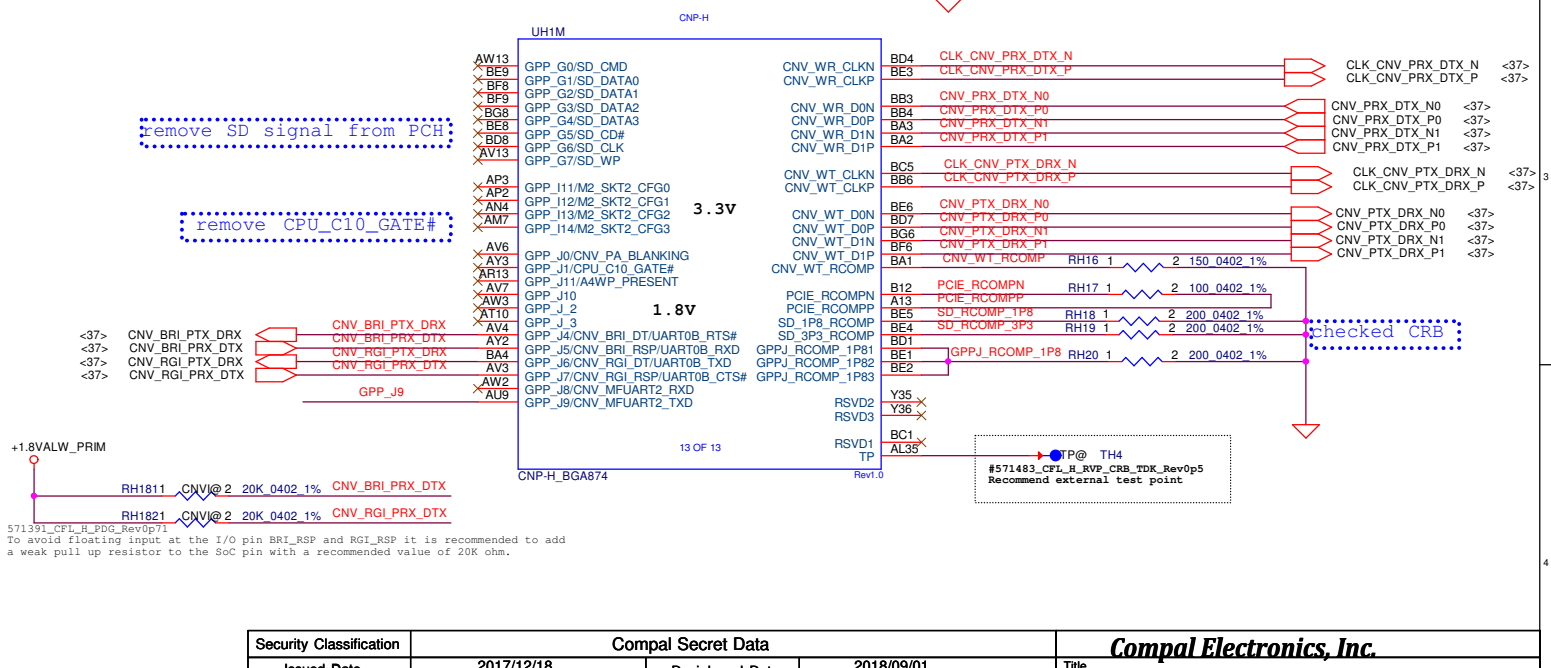
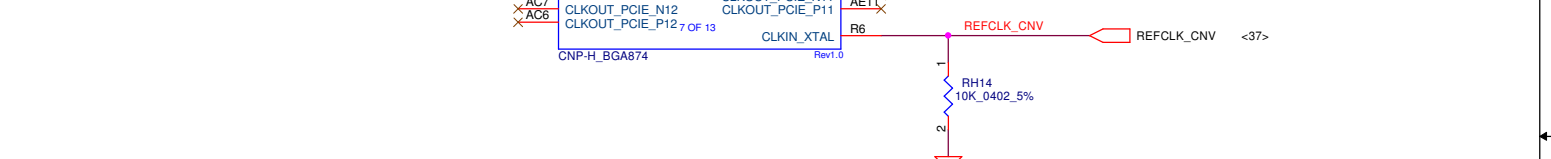
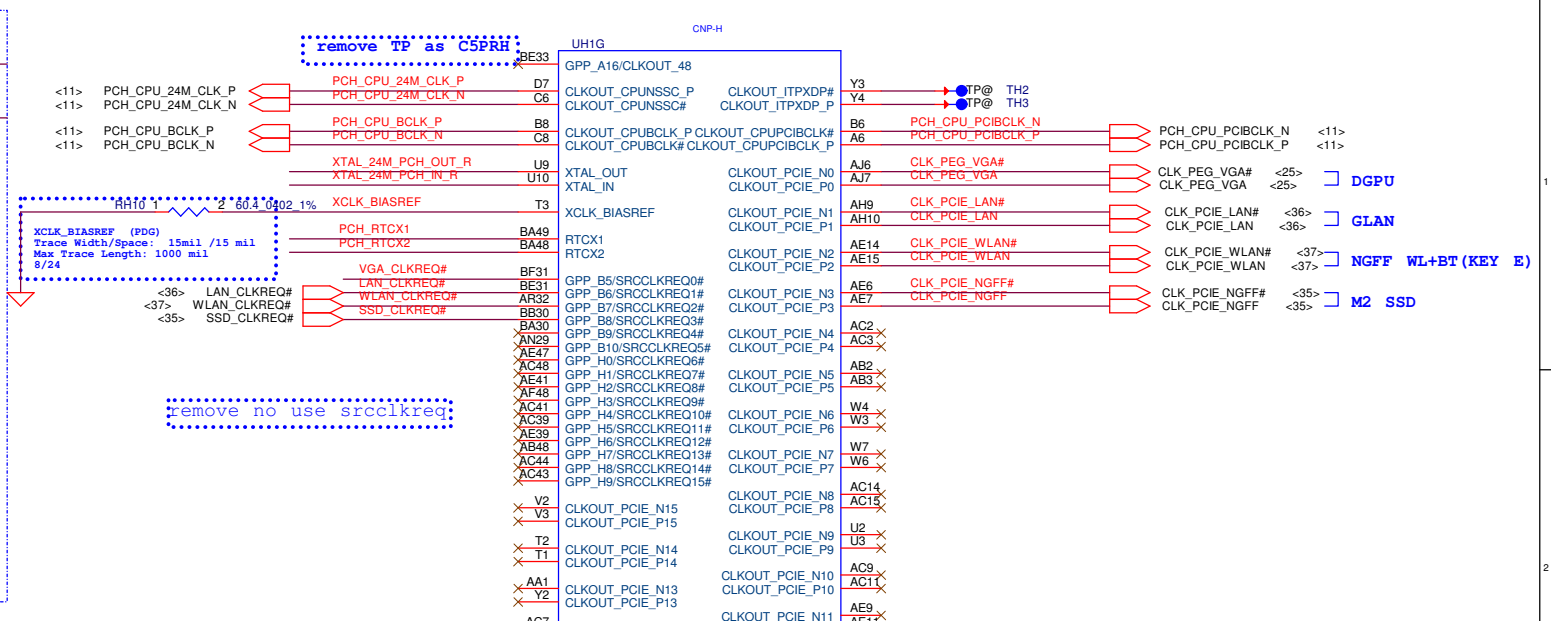


CFL-H (HM370)		Compal	
Lane0	USB3.1 Port1		USB 3 (I/O)
Lane1	USB3.1 Port2		USB 3 Type-C (I/C)
Lane2	USB3.1 Port3		USB 3 Type-C (I/C)
Lane3	USB3.1 Port4		USB 3 (I/O) Daughter Board Reserved
Lane4	USB3.1 Port5		
Lane5	USB3.1 Port6		
Lane6	USB3.1 Port7	PCle Port1	
Lane7	USB3.1 Port8	PCle Port2	
Lane8	USB3.1 Port9	PCle Port3	
Lane9	USB3.1 Port10	PCle Port4	
Lane10		PCle Port5	
Lane11		PCle Port6	
Lane12		PCle Port7	
Lane13		PCle Port8	
Lane14		PCle Port9	M.2 SSD#1 (PCle x4)
Lane15		PCle Port10	M.2 SSD#1 (PCle x4)
Lane16	SATA3 Port0	PCle Port11	M.2 SSD#1 (PCle x4)
Lane17	SATA3 Port1	PCle Port12	M.2 SSD#1 (PCle x4)
Lane18	SATA3 Port0*	PCle Port13	
Lane19	SATA3 Port1*	PCle Port14	LAN+CR
Lane20	SATA3 Port2	PCle Port15	WIFI
Lane21	SATA3 Port3	PCle Port16	
Lane22	SATA3 Port4	PCle Port17	HDD
Lane23	SATA3 Port5	PCle Port18	
Lane24		PCle Port19	
Lane25		PCle Port20	
Lane26		PCle Port21	
Lane27		PCle Port22	
Lane28		PCle Port23	
Lane29		PCle Port24	
	USB2 Port1		USB 3 (I/O)
	USB2 Port2		USB 3 Type-C (I/C)
	USB2 Port3		USB 2 (I/O)
	USB2 Port4		USB 2 (I/O)
	USB2 Port5		CCD
	USB2 Port6		TS
	USB2 Port7		
	USB2 Port8		FP
	USB2 Port9		
	USB2 Port10		
	USB2 Port11		
	USB2 Port12		
	USB2 Port13		
	USB2 Port14		BT

Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					
	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	PCle* #1	USB3.1 #8	PCle* #2	USB3.1 #9	PCle* #3	USB3.1 #10	PCle* #4	PCle* #5	PCle* #6	PCle* #7	PCle* #8	PCle* #9	PCle* #10	PCle* #11	PCle* #12	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	PCle* #18	PCle* #19	PCle* #20	PCle* #21	PCle* #22	PCle* #23	PCle* #24
High Speed I/O (HSIO) Type and Lane																																			
Intel® RST Support											No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	PCH(1/8)DMI/PCIE/USB2
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				Date:	Thursday, February 22, 2018
				Sheet	15 of 67



Security Classification		Compal Secret Data		Compal Electronics, Inc. PCH(2/8)CLK/CNV1/SD	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Customer	Document Number
				DH5VF M/B LA-F591PR01	
Date: Thursday, February 22, 2018				Sheet 16 of 67	

can remove if no use DP
08/18

remove PCH DP SCLK/SDATA

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B-D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after
PCH_PWRON de-asserts.
2. This signal is in the primary well.

no follow naming

<25,34> HDMI_HPD_PCH

<25,33> EDP_HPD

<36,39>

EC_PME#

RH24

EC_PME#_R

BE36

TP@

0.0402_5%

1

2

0.0402_5%

2

0.0402_5%

1

1K

0.0402_5%

1

1K

0.0402_5%

1

1K

0.0402_5%

1

1K

0.0402_5%

1

1K

0.0402_5%

1

1K

0.0402_5%

1

1K

0.0402_5%

* wait confirm CG7

PDG_P348 quad mode support PH1K

CRB PU 20k

#571182_CFL_PCH_EDS_Rev1.0 recommend 100k

#571391_CFL_PCH_EDS_Rev0p71

RH25 2 1 1K 0.0402_5% PCH_SPL_IO2

RH26 2 1 1K 0.0402_5% PCH_SPL_IO3

RH27 2 1 1K 0.0402_5% PCH_SPL_SI

RH29 2 1 100K 0.0402_5% GPP_H15 STRAP

#571182_CNL_PCH_H_EDS_V1_Rev0.7

External pull-up is required. Recommend 100K if pulled

up to 3.3V or 75K if pulled up to 1.8V.

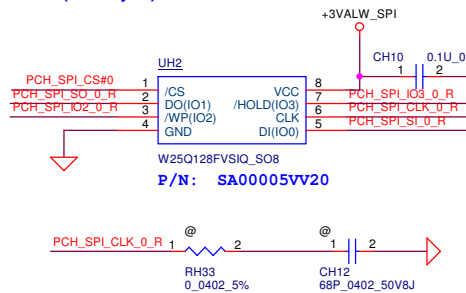
571007_CFL_MOM_Archive_MW22_2017

STUFF R on GPP_H15

PCH_SPL_CLK RH1951 2 100K 0.0201_5%

intel critical net recommend

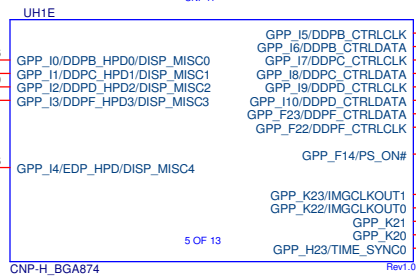
SPI ROM (16MByte)



note : 1050 Use 8M rom

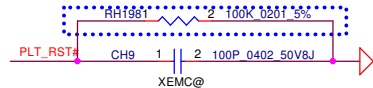
PCH_SPL_SI_0_R	RH107	1	2	49.9	0.0402	1%	PCH_SPL_SI
PCH_SPL_SO_0_R	RH108	1	2	49.9	0.0402	1%	PCH_SPL_SO
PCH_SPL_IO3_0_R	RH109	1	2	49.9	0.0402	1%	PCH_SPL_IO3
PCH_SPL_CLK_0_R	RH110	1	2	49.9	0.0402	1%	PCH_SPL_CLK
PCH_SPL_IO2_0_R	RH111	1	2	49.9	0.0402	1%	PCH_SPL_IO2

sch checklist 0.7
1 device 15 ohm / 2 device 33 ohm



remove CIO_PLUGIN_EVENT#

intel critical net recommend



GPIO Serial Expander (GSX) is the capability
provided by the PCH to expand the GPIOs
on a platform that needs more GPIOs than the
ones provided by the PCH.

TP_INT# 2 1
TYPEPEC_1P5A DH1
RB751V40_SOD323-2

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

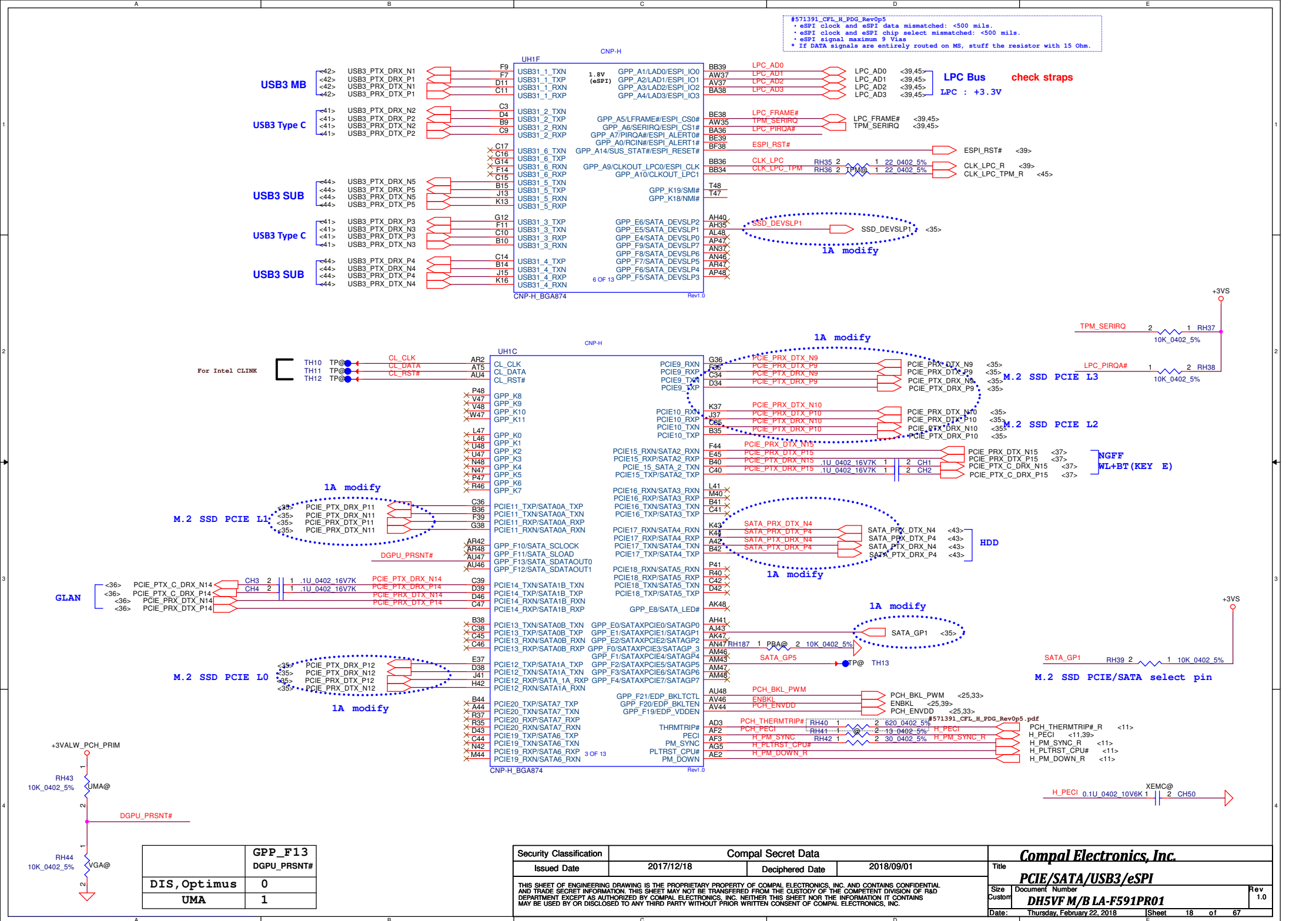
TP_INT# RH28 2 1 100K 0.0402_5%

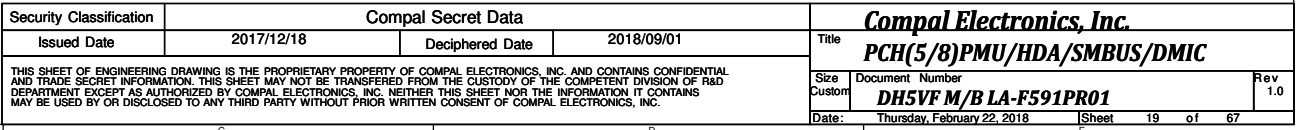
TP_INT# RH28 2 1 100K 0.0402_5%

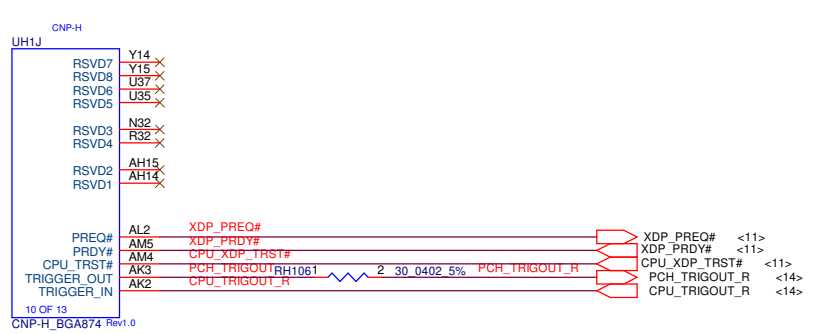
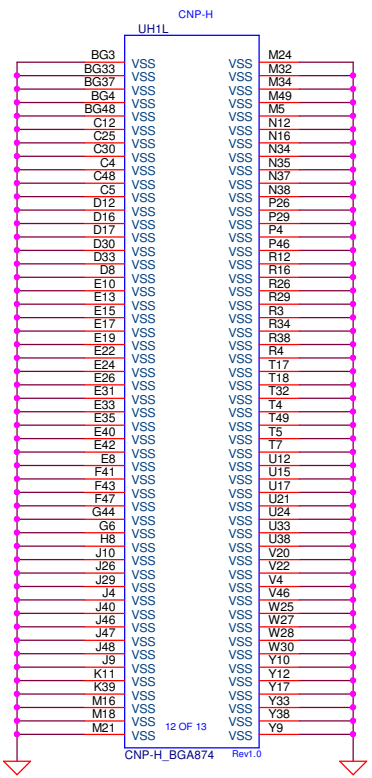
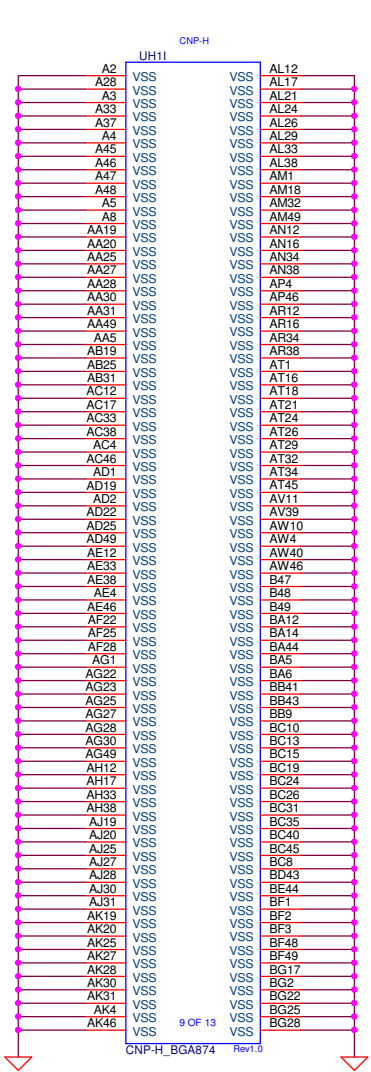
TP_INT# RH28 2 1 100K 0.0402_5%

TP_INT# RH28 2 1 100K 0.0402_5%

Security Classification	Compal Secret Data	Title	
Issued Date	2017/12/18	Deciphered Date	
2018/09/01		2018/09/01	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			
Size	Document Number	Rev	
Custom	DH5VF M/B LA-F591PR01	1.0	
Date:	Thursday, February 22, 2018	Sheet	17 of 67







Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2017/12/18		Deciphered Date		2018/09/01		Title	
										PCH(8/8)GND/RSVD	
										Size	
										Document Number	
										DH5VF M/B LA-F591PR01	
										Date:	
										Thursday, February 22, 2018	
										Sheet	
										22 of 67	
										Rev	
										1.0	

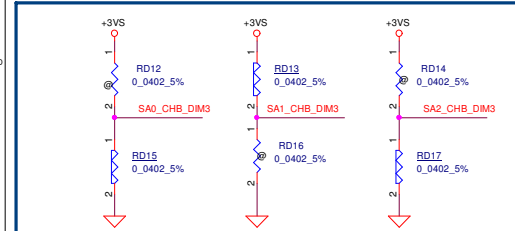
CHANNEL-B

BOT

STD (4 mm)

Interleaved Memory

TOP: JDIMM3 CONN Non-ECC DIMM

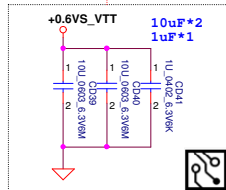
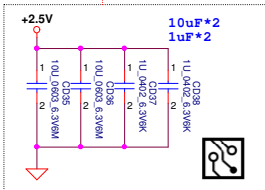


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

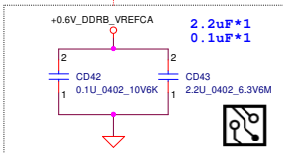
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM3.257,259

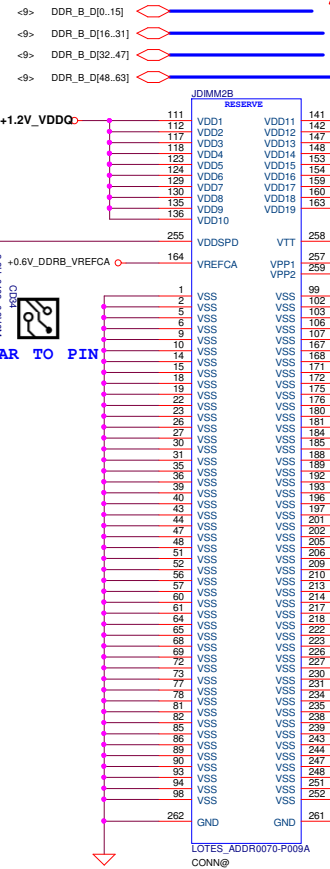
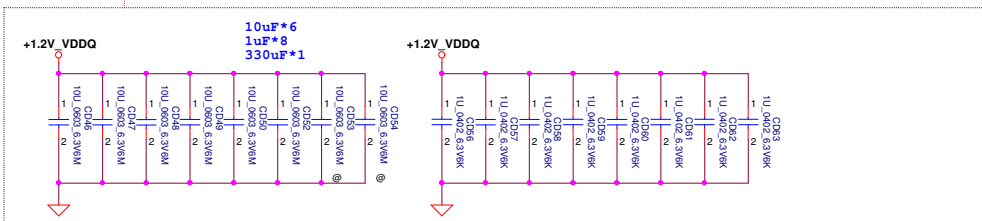
Layout Note:
Place near JDIMM3.258



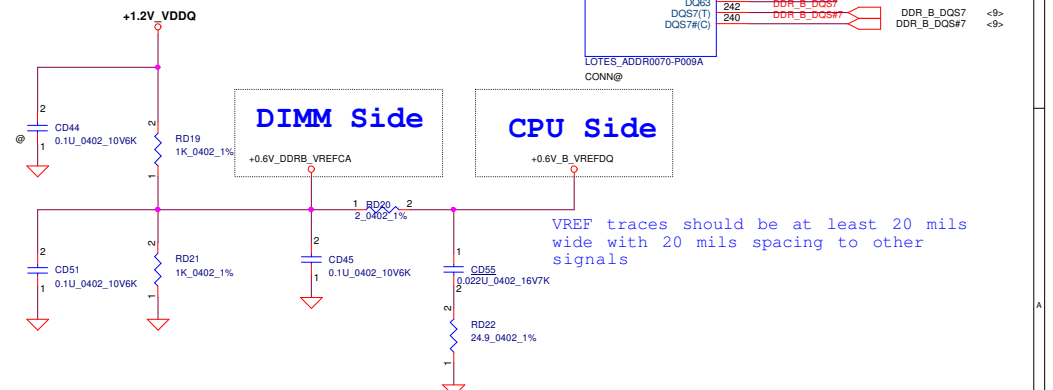
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



Layout Note:
Place near JDIMM3



Part Number:SP07001CEA0
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4



VREF traces should be at least 20 mils
wide with 20 mils spacing to other
signals

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
				DDRIV_CHB: DIMM0	
				Size	Document Number
				DH5VF M/B LA-F591PR01	
				Date:	Thursday, February 22, 2018
				Sheet	24 of 67

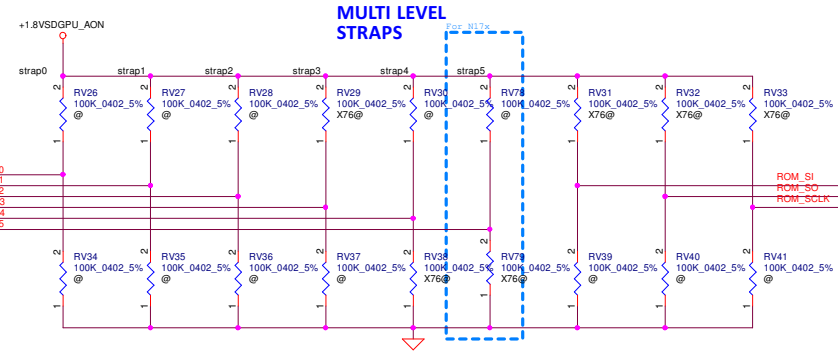
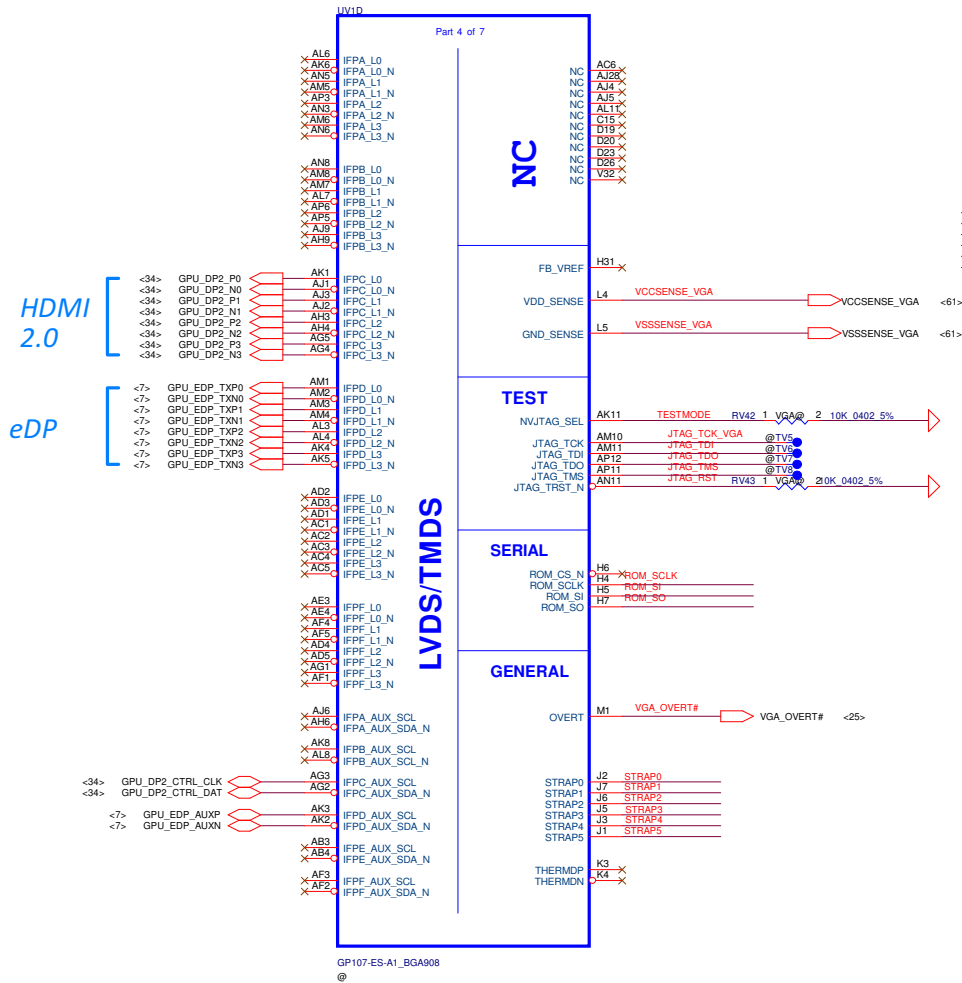


Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V ²	Samsung	K4G80325F3-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325F3-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver ³
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver ³
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver ³
4 Gb	128Mx32	1.35V and 1.5V ²	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver ³
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver ³

Strap Pins Note 1

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	0
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ATT_ADDR	
LOW	Single GPU
High	Dual GPU
DEVID_SEL	
LOW	Orig. Device ID
High	Support G-Sync GPUID
VGA_DEVICE	
LOW	3D Device
High	VGA Device
PCIE_CFG	
LOW	Normal signal swing
High	Reduce the signal amplitude

Table 5.2 RAMCFG

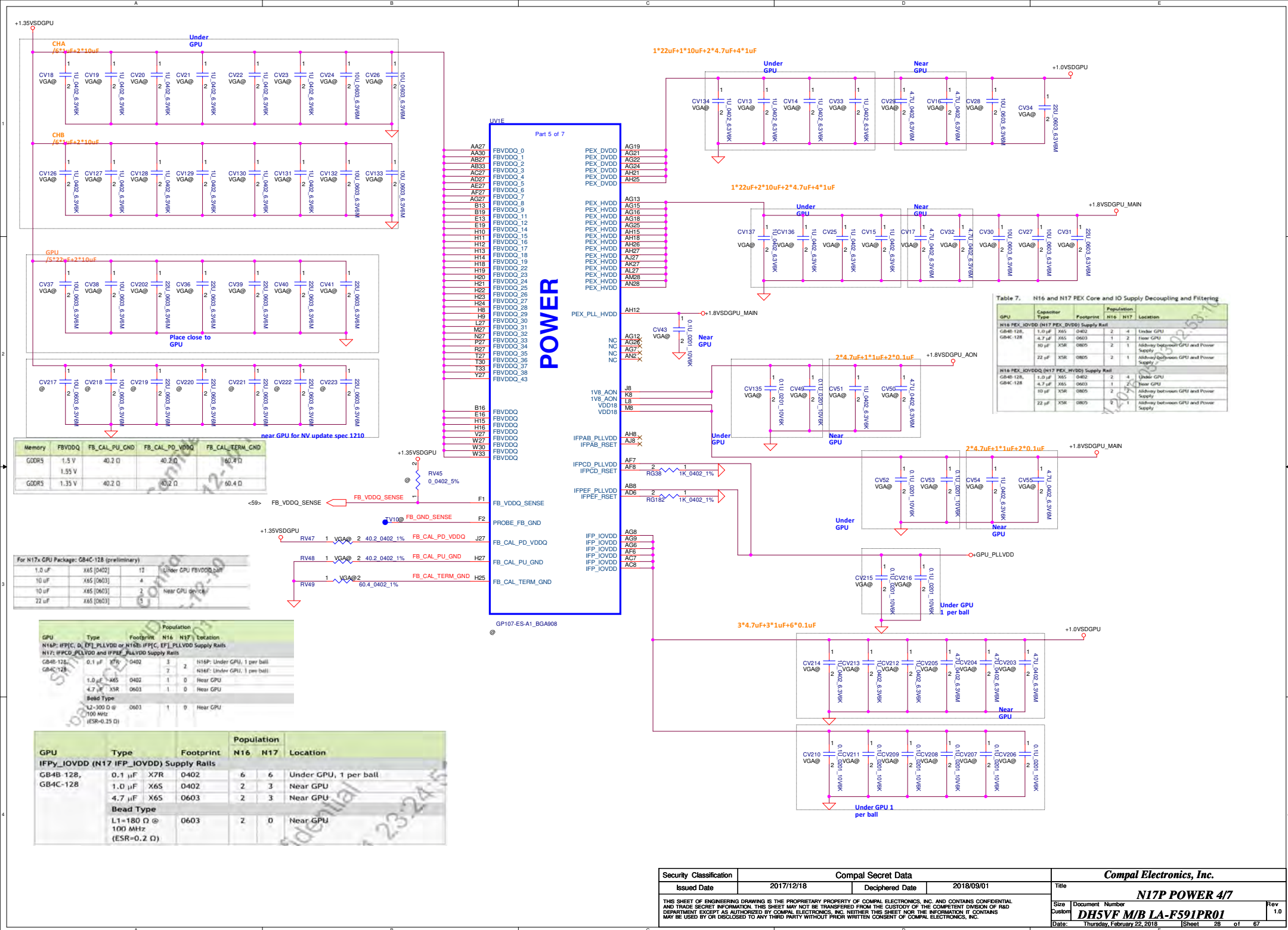
Strap Pins We Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
L	H	L	12 (0x000C)
M	L	L	13 (0x000D)

Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins <small>see Note</small>			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
U	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			

HDMI audio output

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				N17P STRAP 3/7
Size	Document Number	Rev	Date: Thursday, February 22, 2018	
Custom	DHSVF M/B LA-F591PRO1	1.0	Sheet	27 of 67

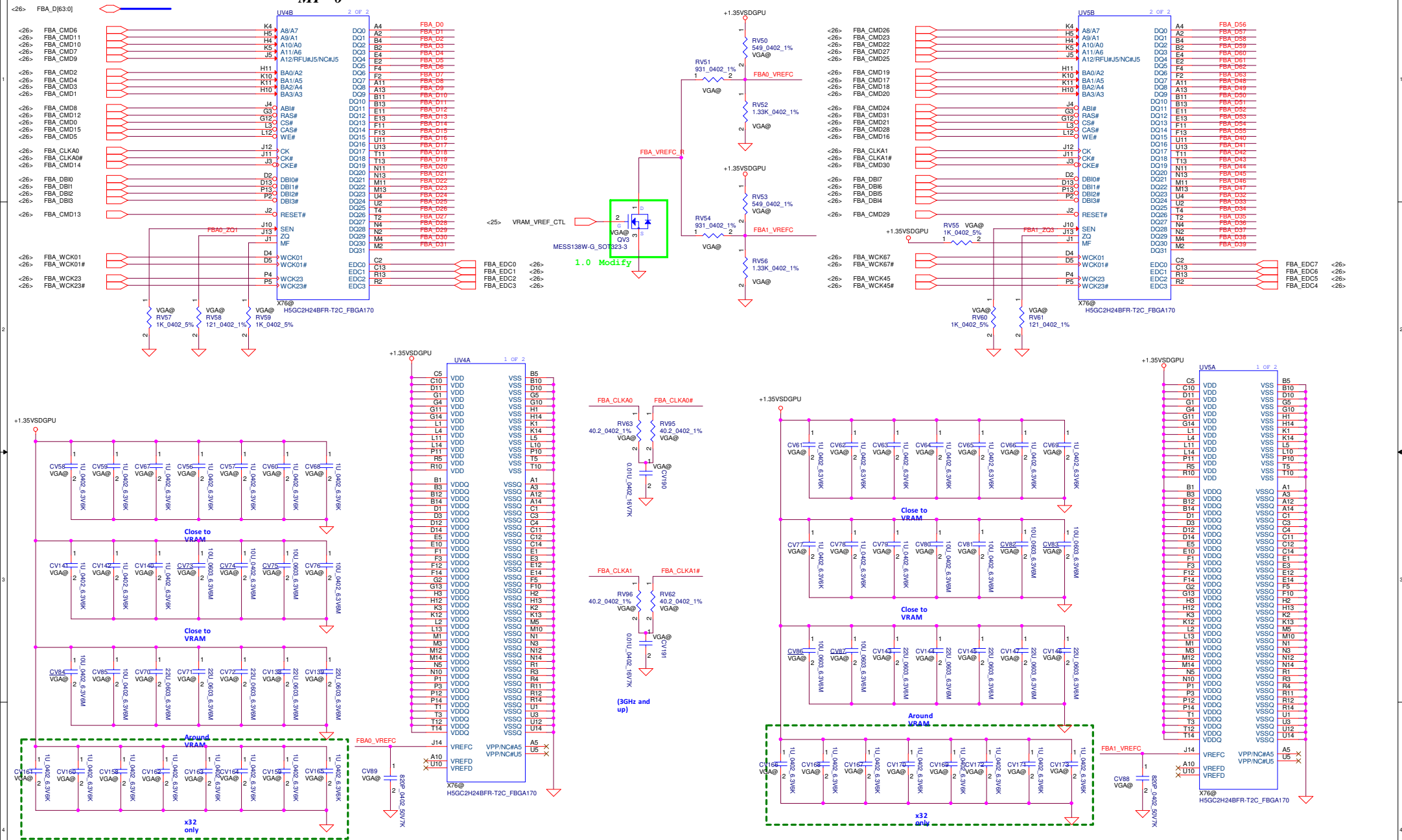


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	N17P POWER 4/7		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev	
				Customer	DH5VF M/B LA-F591PR01		1.0
				Date:	Thursday, February 22, 2018	Sheet	26 of 67

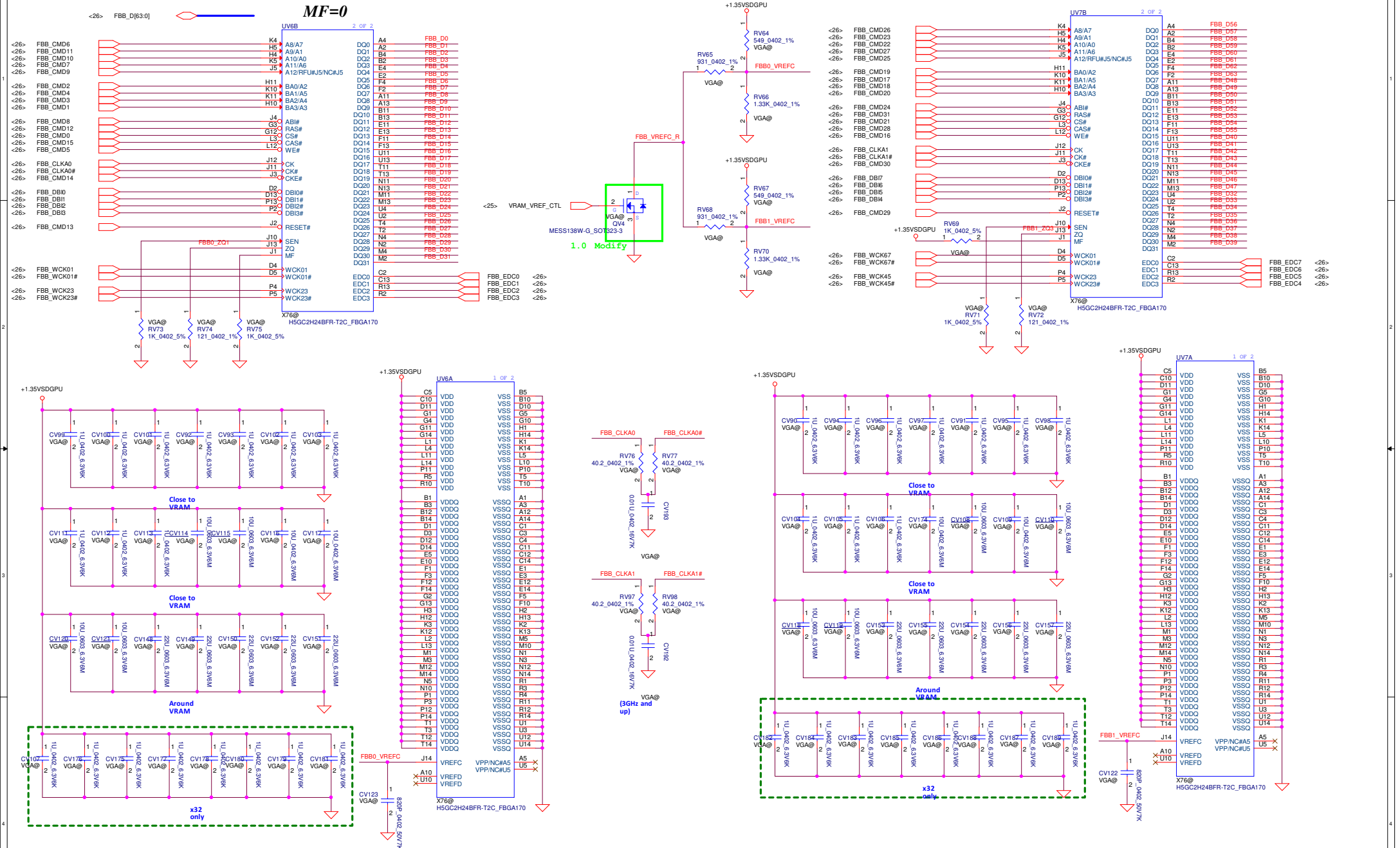
Compal Electronics, Inc.			
Title N17P POWER & GND 5/7			
Size Customer	Document Number DH5VF M/B LA-F591PR01	Rev 1.0	
Date:	Thursday, February 22, 2018	Sheet 29 of 67	

MF=1

MF=0



Security Classification		Compal Secret Data		Title	
Issued Date		2017/12/18		Deciphered Date	
		2018/09/01		Rev	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Date		Thursday, February 22, 2018	
Compal Electronics, Inc.		N17P GDDR5 CHA 6/7		Rev	
Size		Document Number		1.0	
Custom		DHSVF M/B LA-F591PRO1		Sheet	
		30		67	

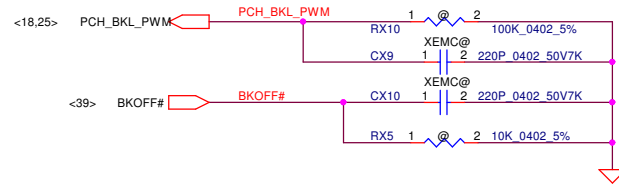
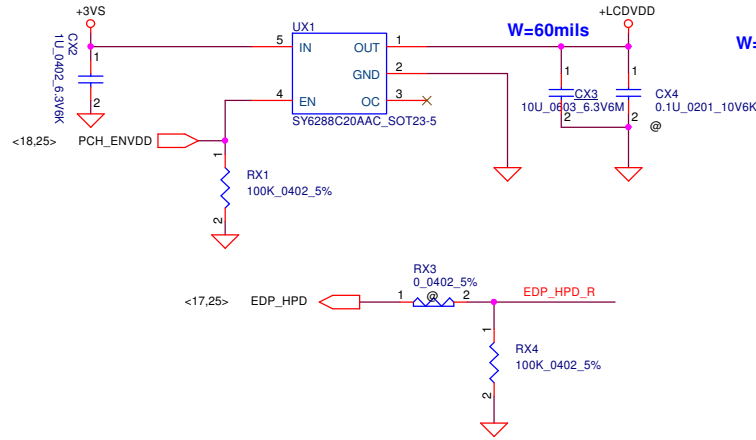
$$MF=1$$
$$MF=0$$


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	N17P GDDR5 CHB 7/7	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev	
				Document Number DH5VF M/B LA-F591PR01	1.0	
Date:	Thursday, February 22, 2018	Sheet	31	of	67	

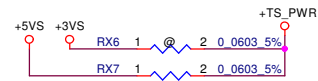
remove GPAK circuit for improve HDMI layout (1.0)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2017/12/18	Deciphered Date	2018/09/01	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		N17P G-Pak sequence 8/8			
		Size Custom	Document Number	Rev 1.0	
		Date:	Thursday, February 22, 2018	Sheet	32 of 67

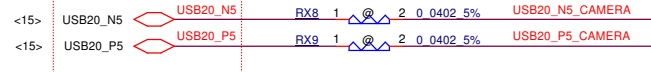
LCD POWER CIRCUIT



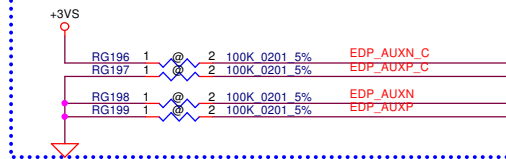
USB Touch Screen



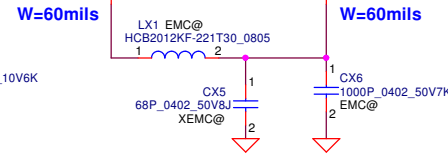
Camera



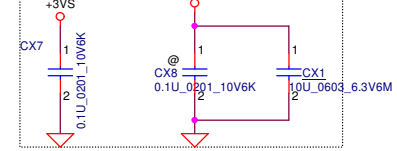
CO-LAY FOR VGA OUTPUT



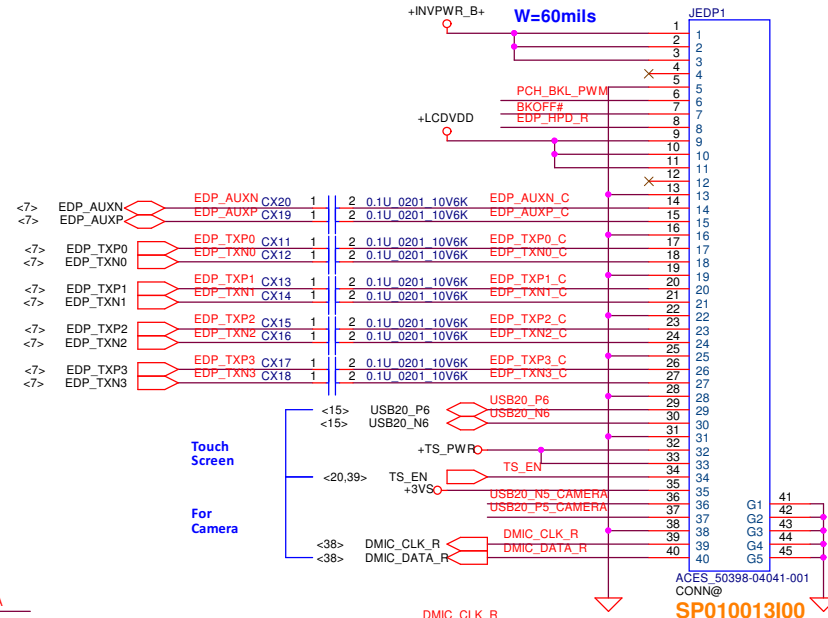
SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04



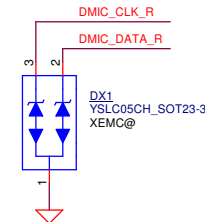
Place closed to JEDP1



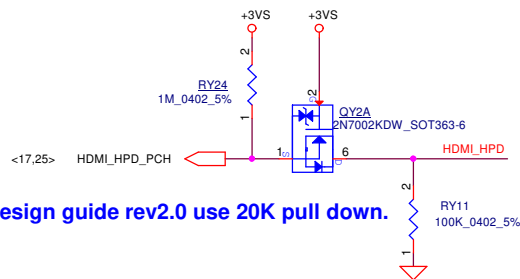
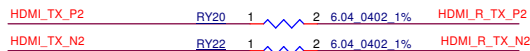
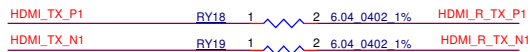
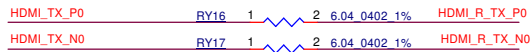
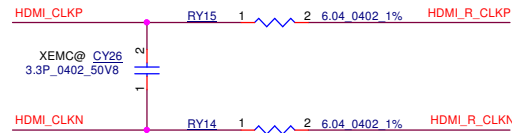
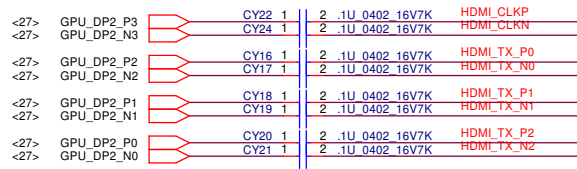
LED PANEL Conn.



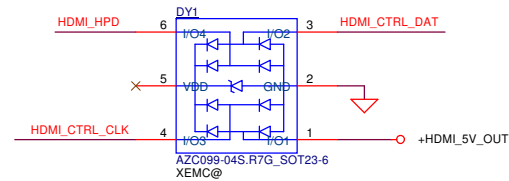
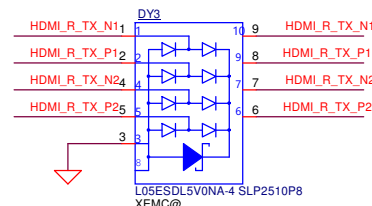
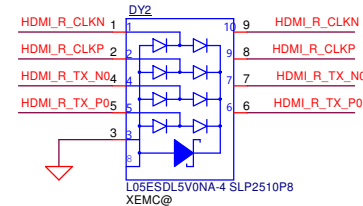
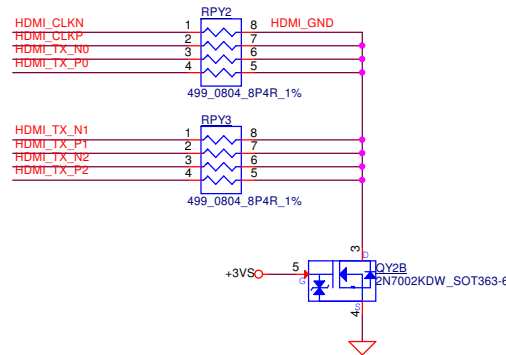
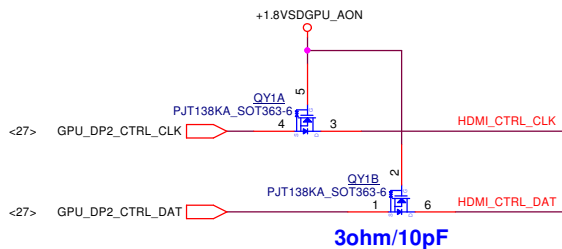
Touch Screen
For Camera



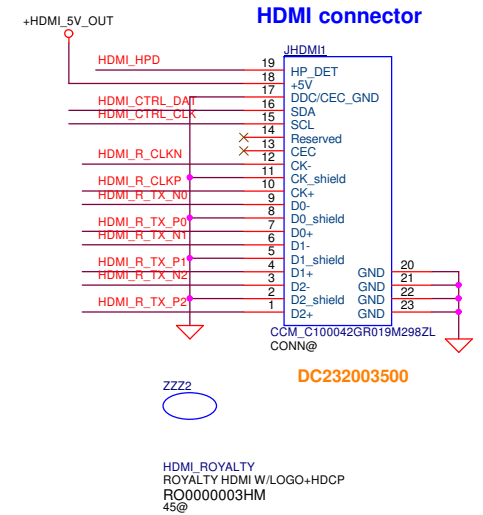
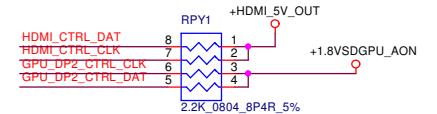
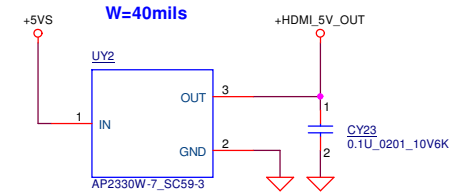
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				eDP CONN.	
Size	Document Number	Rev		1.0	
Custom	DHSVF M/B LA-F591PR01	Date:		Thursday, February 22, 2018	
Sheet		33		of 67	



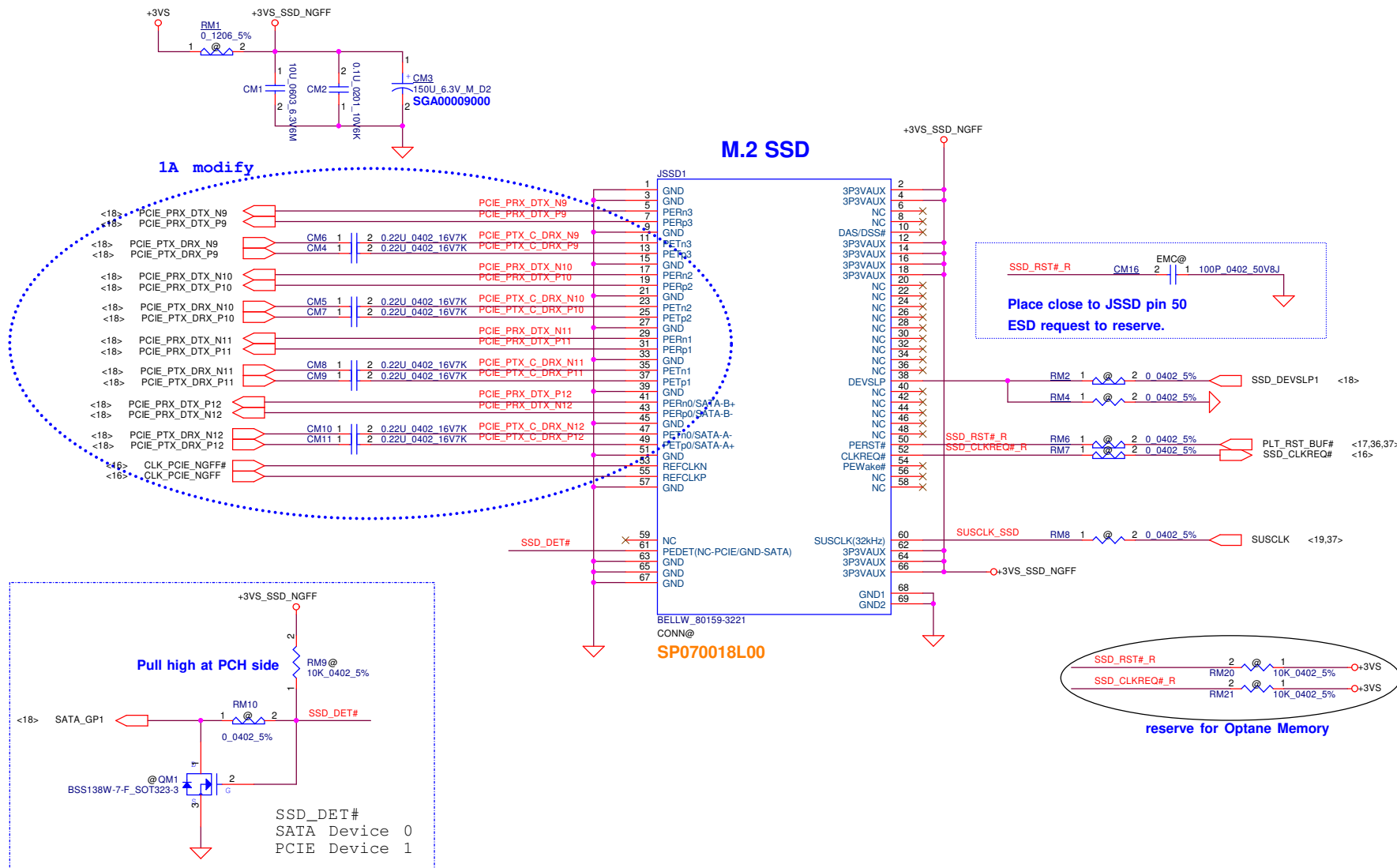
RY11 design guide rev2.0 use 20K pull down.



P/N: SC300002900, S DIO(BR) AZC199-04S.R7G SOT23-6 ESD

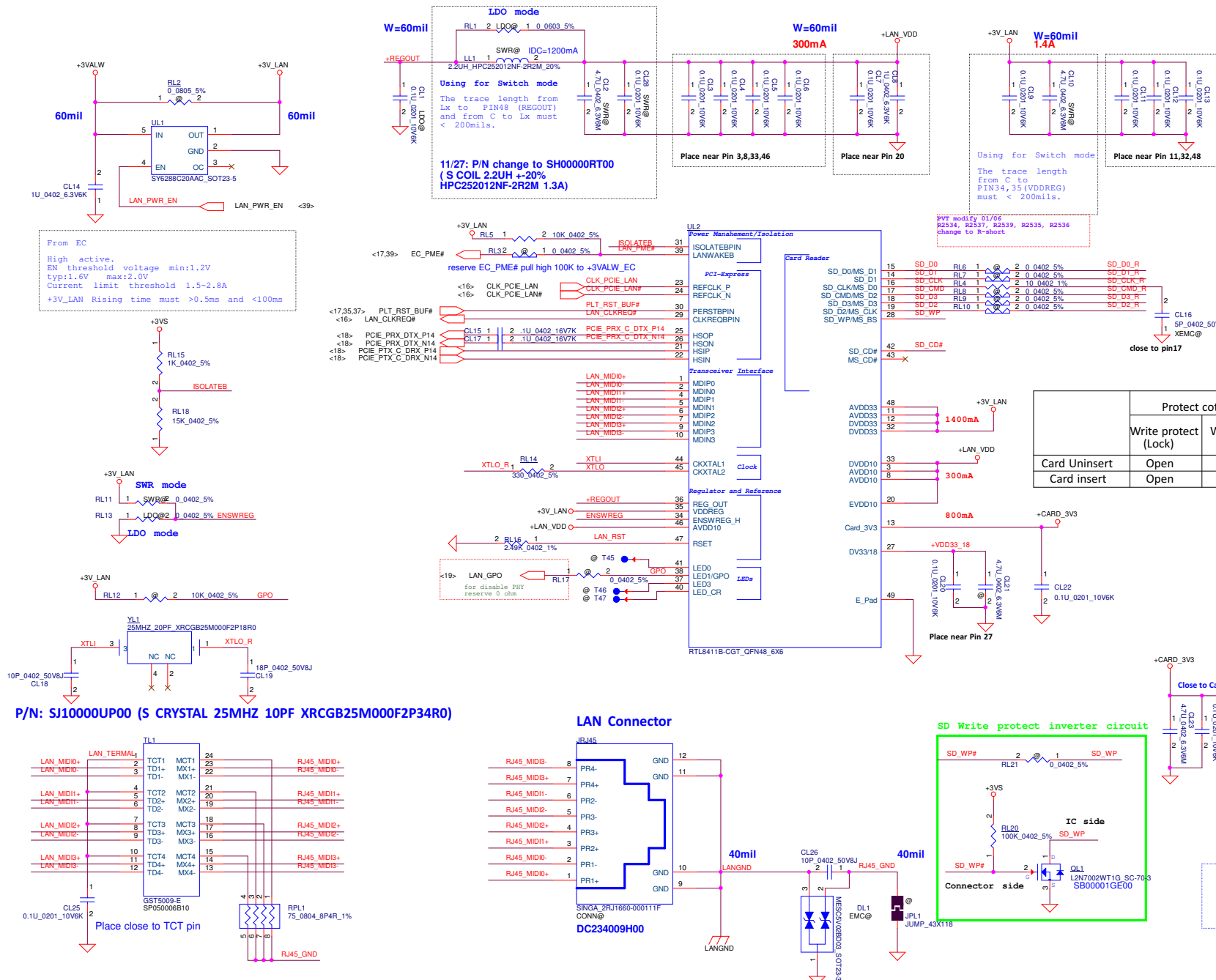


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI CONN.	
Size	Document Number	Date		Sheet	Rev
Custom	DHSVF M/B LA-F591PR01	Thursday, February 22, 2018		34 of 67	1.0

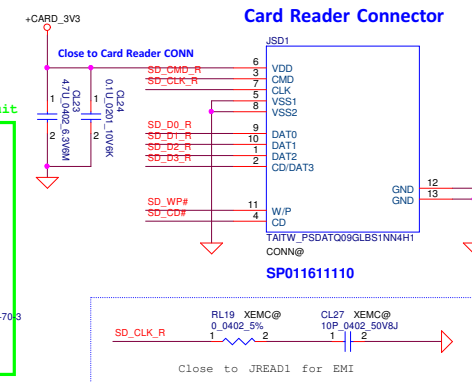


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				mSATA-SSD	
Size	Document Number	Rev		1.0	
Custom	DH5VF M/B LA-F591PR01	Date		Thursday, February 22, 2018	
Sheet		35		of 67	

LAN-RTL8411B

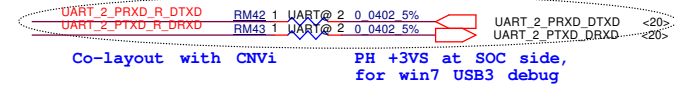
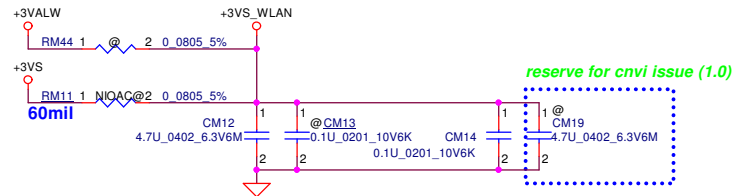
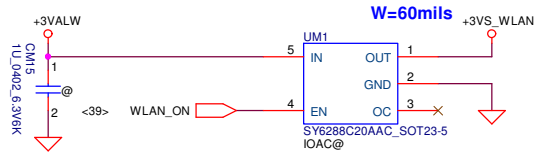


	Protect cotact		Card contac
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

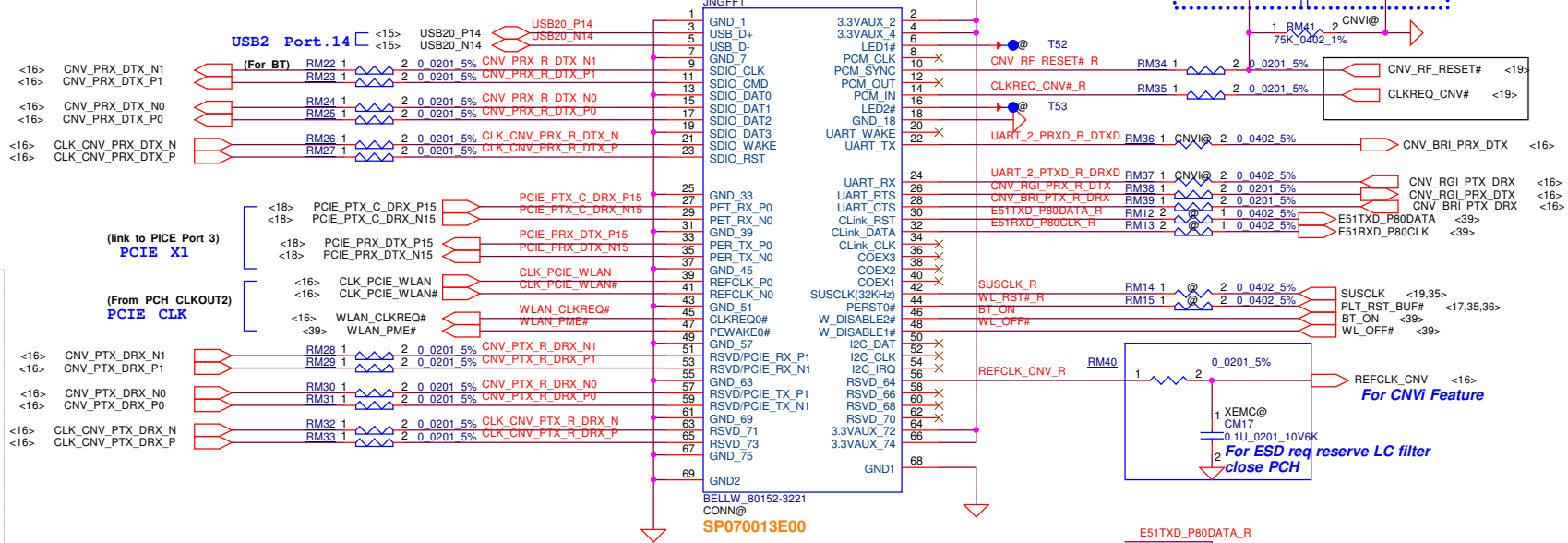


Security Classification		Compal Secret Data		Compal Electronics, Inc. LAN RTL8411H	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	
				Customer	DH5VF M/B LA-F591PR01 Rev 1.0
				Date:	Thursday, February 22, 2018 Sheet 36 of 67

Wireless LAN



KEY E



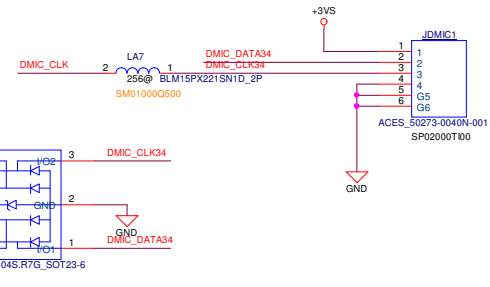
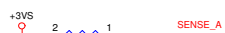
NGFF WL+BT (KEY E)

Pin	Signal	Pin	Signal
74	3VALW	75	3VS_WLAN
72	3VALW	73	3VS_WLAN
70	UM_Power_SRC/GPIO1/PEWake#	71	UM_Power_SRC/GPIO1/PEWake#
68	UM_Power_SRC/CLKREQ0#	69	UM_Power_SRC/CLKREQ0#
66	UM_SWP/PERST#	67	UM_SWP/PERST#
64	RESERVED	65	RESERVED
62	ALERT# (I/O/3.3)	63	ALERT# (I/O/3.3)
60	IO CLK (I/O/3.3)	61	IO CLK (I/O/3.3)
58	IO DATA (I/O/3.3)	59	IO DATA (I/O/3.3)
56	WL_DISABLE# (I/O/3.3V)	57	WL_DISABLE# (I/O/3.3V)
54	Reserved/W_DISABLE2 (I/O/3.3V)	55	Reserved/W_DISABLE2 (I/O/3.3V)
52	PERSTON (I/O/3.3V)	53	PERSTON (I/O/3.3V)
50	SUSCLK (32kHz) (I/O/3.3V)	51	SUSCLK (32kHz) (I/O/3.3V)
48	COEX1 (I/O/1.8V)	49	COEX1 (I/O/1.8V)
46	COEX2 (I/O/1.8V)	47	COEX2 (I/O/1.8V)
44	COEX3 (I/O/1.8V)	45	COEX3 (I/O/1.8V)
42	VENDOR DEFINED	43	VENDOR DEFINED
40	VENDOR DEFINED	41	VENDOR DEFINED
38	VENDOR DEFINED	39	VENDOR DEFINED
36	UART RTS (I/O/1.8V)	37	UART RTS (I/O/1.8V)
34	UART CTS (I/O/1.8V)	35	UART CTS (I/O/1.8V)
32	UART TX (I/O/1.8V)	33	UART TX (I/O/1.8V)
22	UART RX (I/O/1.8V)	23	UART RX (I/O/1.8V)
20	UART Wake# (I/O/3.3V)	21	UART Wake# (I/O/3.3V)
18	IO DATA (I/O/1.8V)	19	IO DATA (I/O/1.8V)
16	IO DATA (I/O/1.8V)	17	IO DATA (I/O/1.8V)
14	IO DATA (I/O/1.8V)	15	IO DATA (I/O/1.8V)
12	IO DATA (I/O/1.8V)	13	IO DATA (I/O/1.8V)
10	IO DATA (I/O/1.8V)	11	IO DATA (I/O/1.8V)
8	IO DATA (I/O/1.8V)	9	IO DATA (I/O/1.8V)
6	IO DATA (I/O/1.8V)	7	IO DATA (I/O/1.8V)
4	IO DATA (I/O/1.8V)	5	IO DATA (I/O/1.8V)
2	IO DATA (I/O/1.8V)	3	IO DATA (I/O/1.8V)

http://www.compel.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	M.2 Key E (WLAN)
THIS IS A LIST OF ENGINEERING DRAWING IS THE PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, WITHOUT PERMISSION IN WRITING FROM COMPAL ELECTRONICS, INC. ANY UNAUTHORIZED REPRODUCTION OR DISCLOSURE OF THIS INFORMATION IS STRICTLY PROHIBITED AND WILL BE PUNISHED BY LAW.				Size	Document Number
				Custom	DHSVF M/B LA-F591PR01
				Date	Thursday, February 22, 2018
				Sheet	37 of 67
				Rev	1.0

2000mA 600ohm@100MHz

[illegible]

MIC BOM upload by Audio Team



TO IO/B

MIC2_VREF0

RA15 1 2 2.2K_0402 5% SLEEVE SLEEVE <44>

RA18 1 2 2.2K_0402 5% RING2 RING2 <44>

HP_LEFT RA20 1 2 0.0603 5% HPOUT_L_1 HPOUT_L_1 <44>

HP_RIGHT RA21 1 2 0.0603 5% HPOUT_R_1 HPOUT_R_1 <44>

LINE1_L CA23 1 2 4.7U_0402 6.3V6M

LINE1_R CA24 1 2 4.7U_0402 6.3V6M

DA3

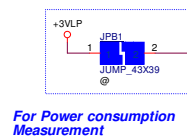
RA23 1 2 4.7K_0402 5%

RA28 1 2 4.7K_0402 5%

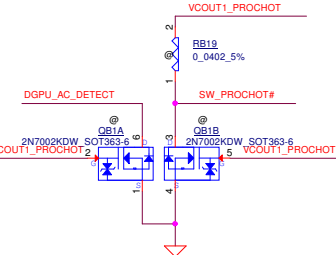
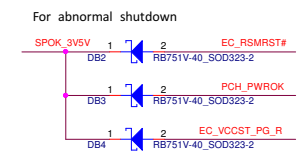
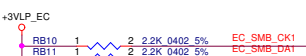
BAT54A7-F SOT23-3

SCSBAT54100

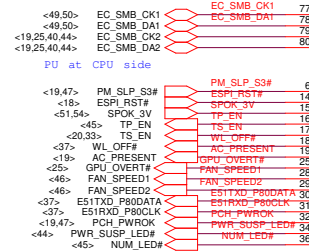
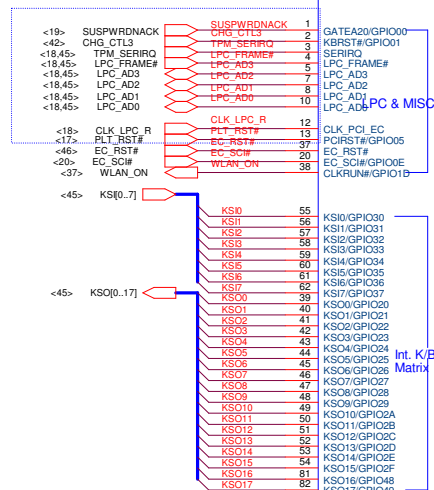
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	HD Audio Codec ALC255	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	DH5VF M/B LA-F591PR01	1.0
				Date:	Thursday, February 22, 2018	Sheet 38 of 67



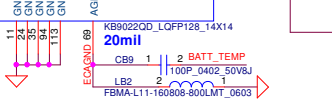
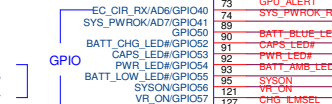
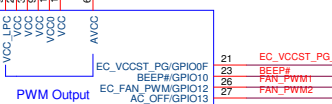
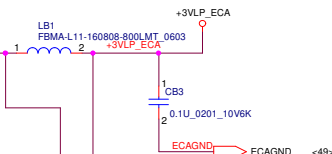
For Power consumption Measurement



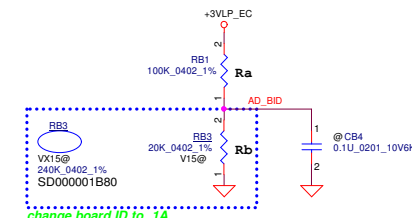
Remove CNVI detect pin on EC(1.0)



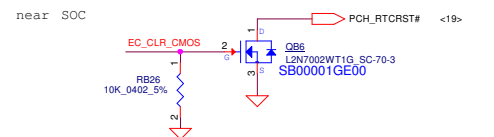
CO-LAY with KB9032QA (SA000080J00)



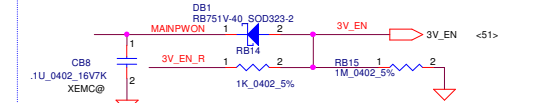
2015/1/9 acer require:
reserved protect circuit when
adaptor 107% happen



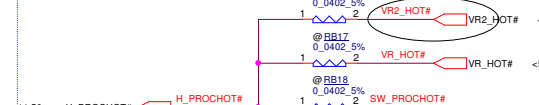
**Analog Board ID definition,
Please see page 3.**



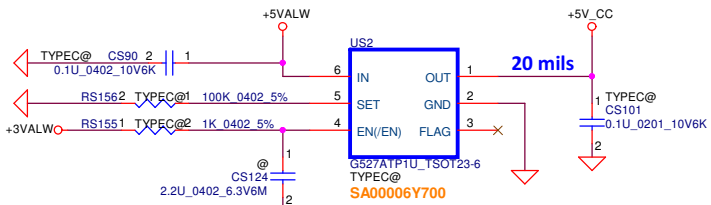
For Thermal Protect Shutdown



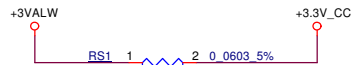
[@RB74](#) [FOLLOW TD](#)



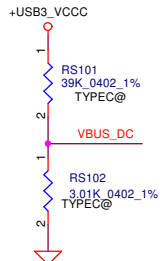
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	EC ENE-KB9012A4/KB9022
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Customer	DH5VF M/B LA-F591PR01
				Date:	Thursday, February 22, 2018
				Sheet	39 of 67



0.2A OCP for VCONN!

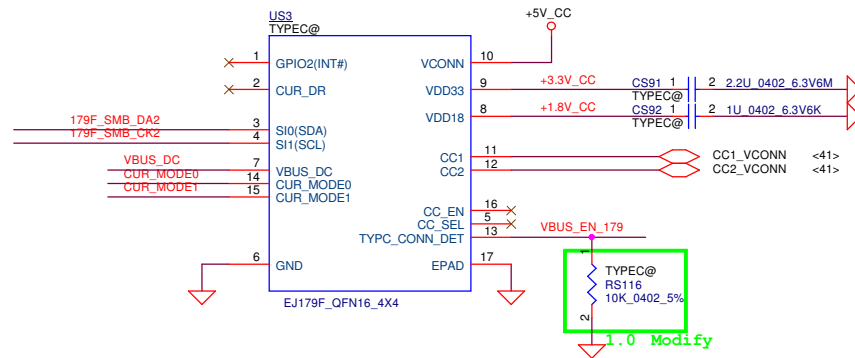


1.0 Modify

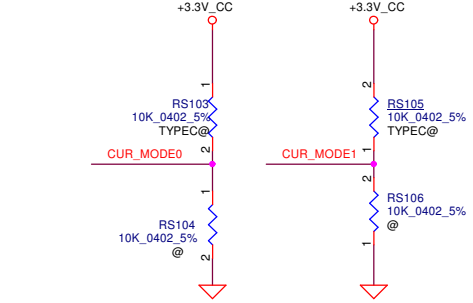


Scaled input
for detection of VBUS DC levels

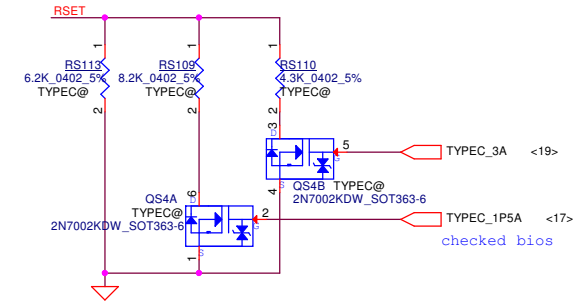
Remove INI#,
platform doesn't monitor it
report CC1 or CC2 is connection
CC_EN
power path control "low active"



1.0 Modify

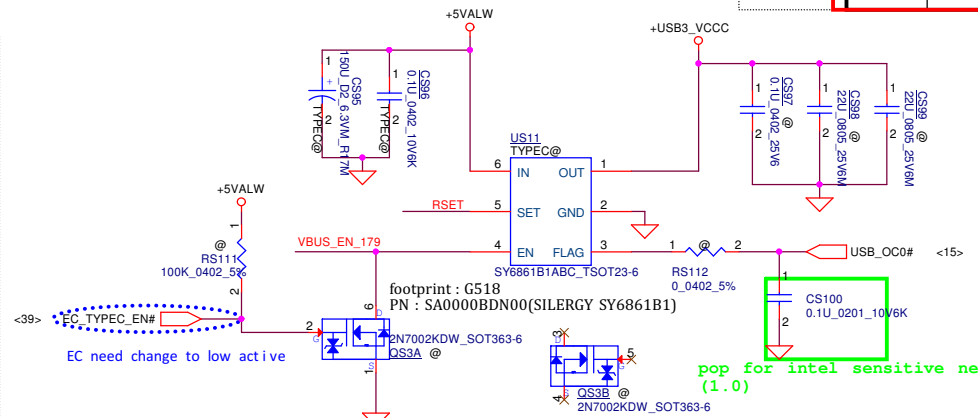
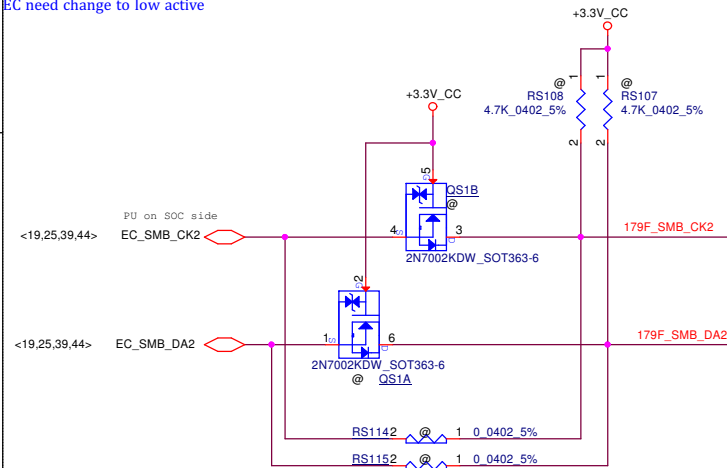


Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current



G518 MOS Current Limit				
GPP_B1 (TYPEC_3A)	GPP_B4 (TYPEC_1P5A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
H	H	1.94	3A	3.5A

EC need change to low active

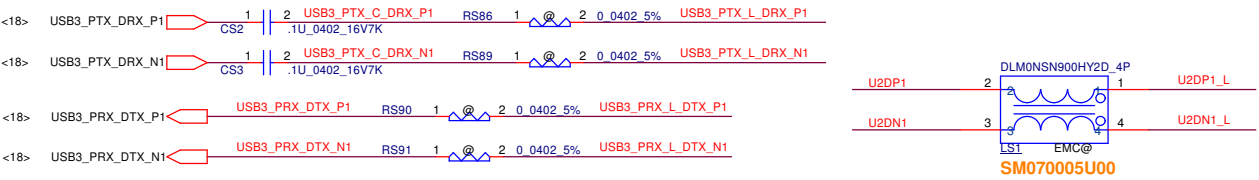


EC need change to low active

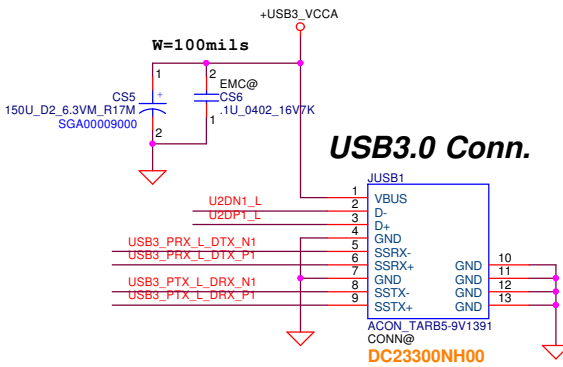
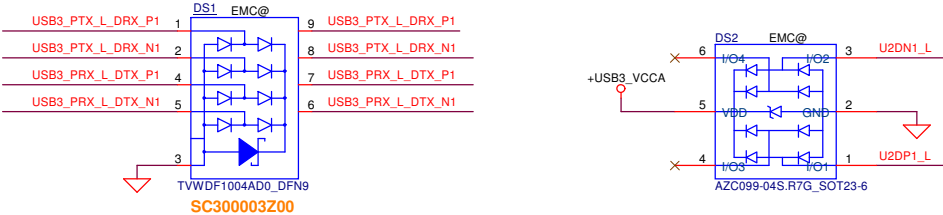
pop for intel sensitive net
(1.0)

Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

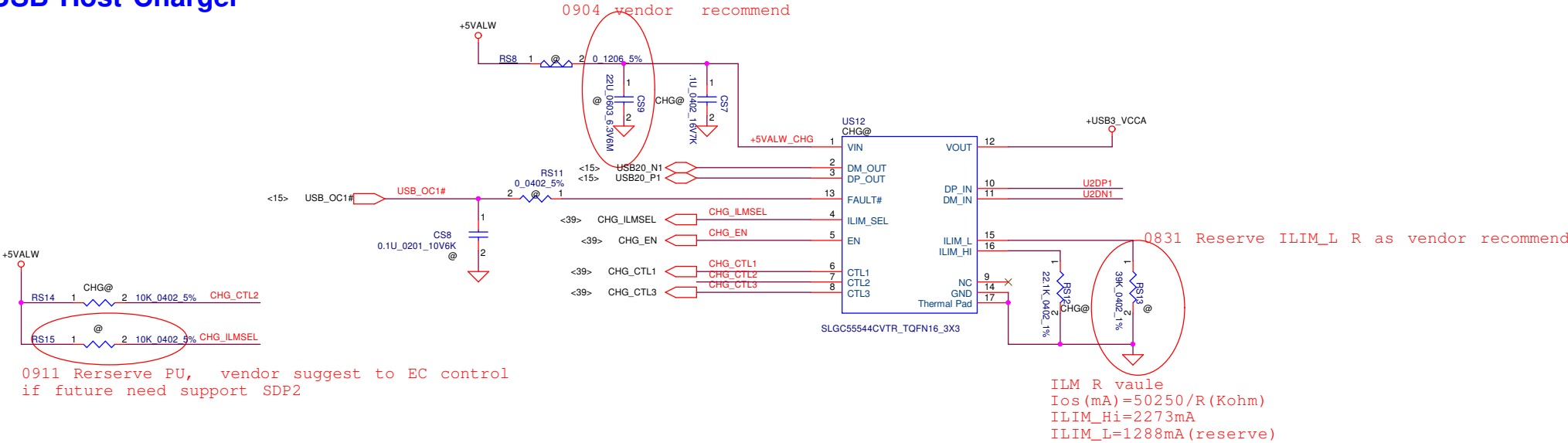
USB3.0 /2.0 CMC



ESD request



USB Host Charger

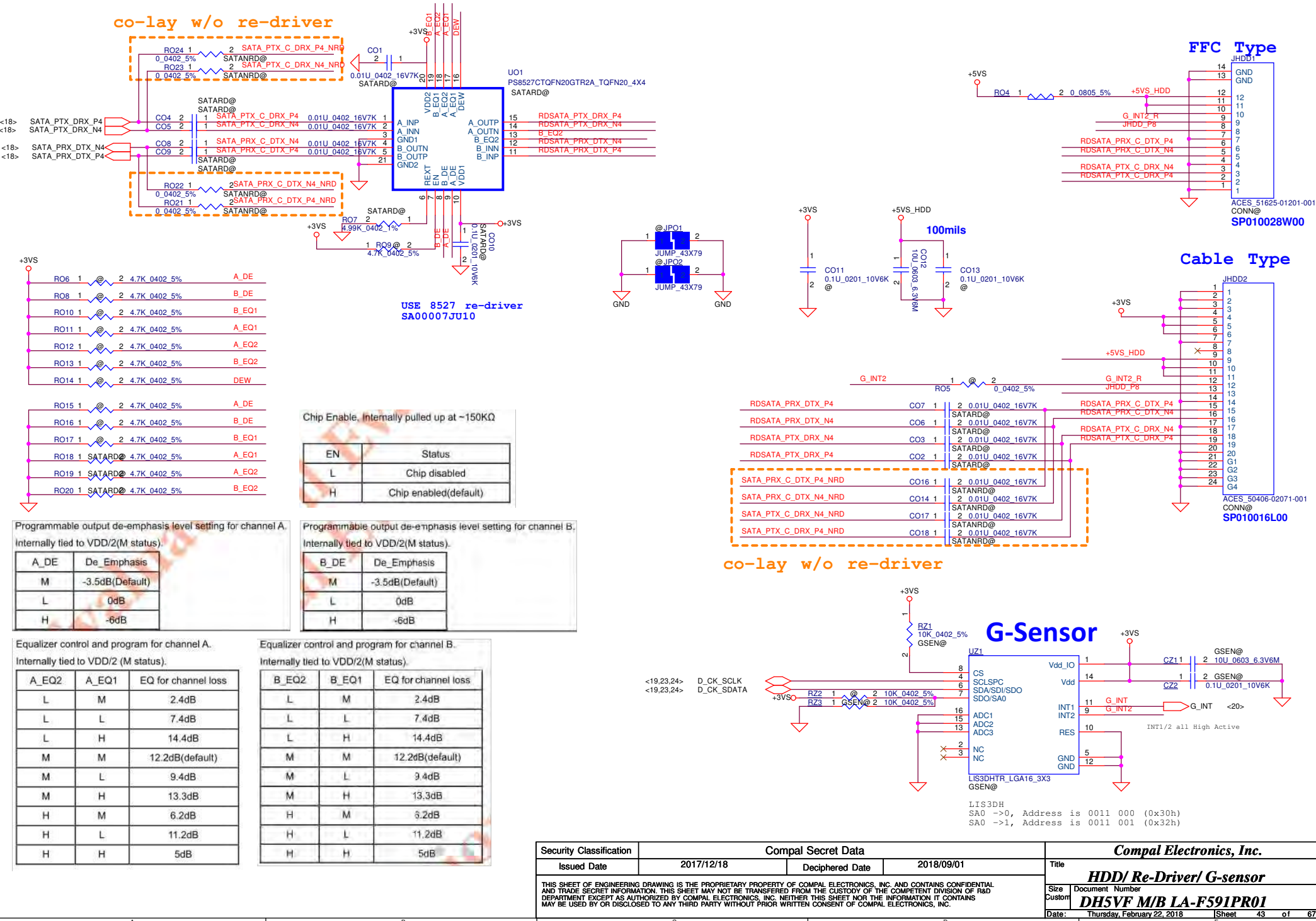


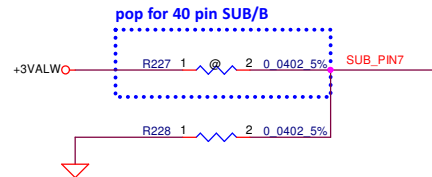
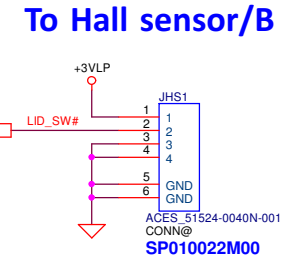
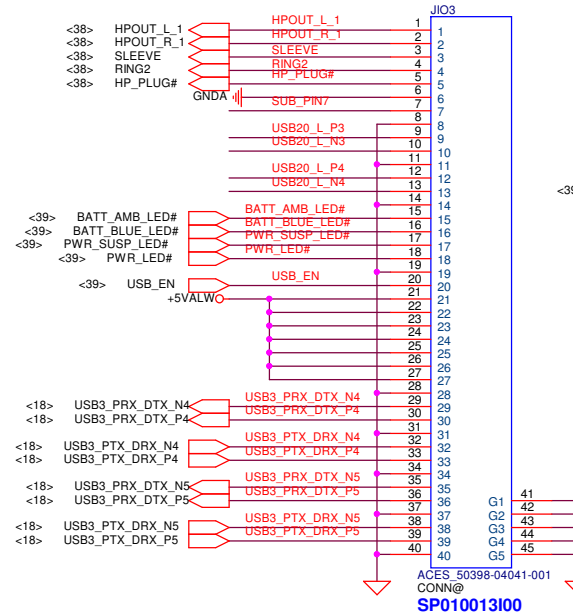
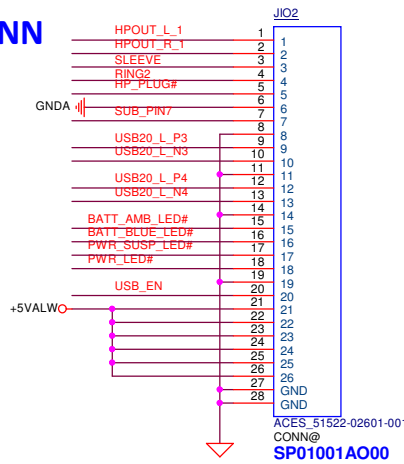
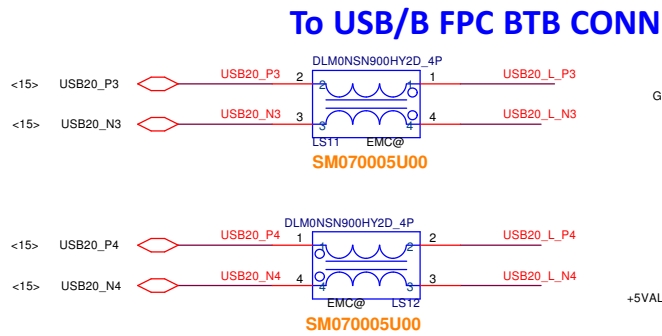
USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

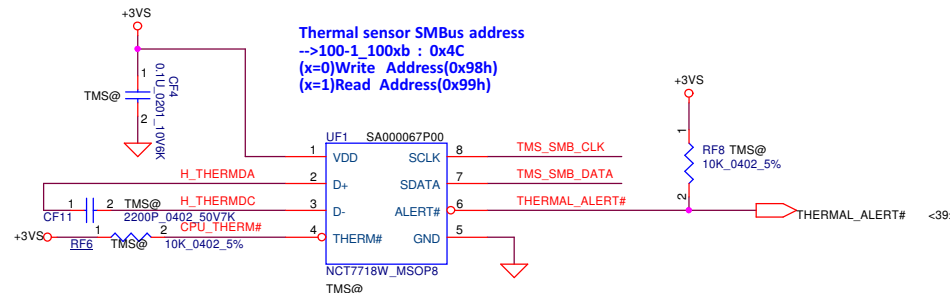
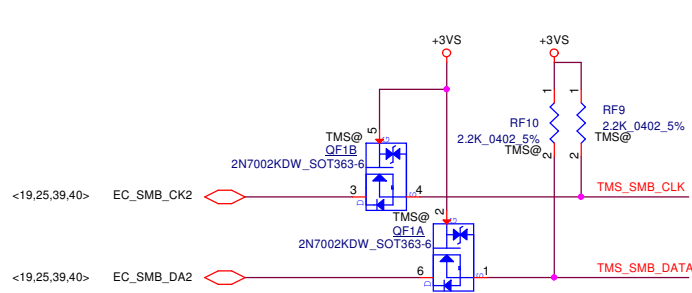
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2017/12/18		Deciphered Date		2018/09/01		Title			
								USB3.0 Conn/USB Charger			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Size	Document Number	Rev	1.0
Date:		Thursday, February 22, 2018						Sheet	42	of	67

SATA Re-Driver and cable HDD Conn.



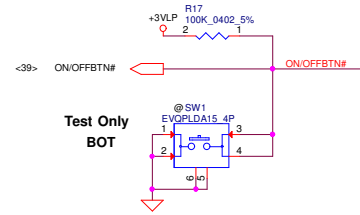


THERMAL SENSOR

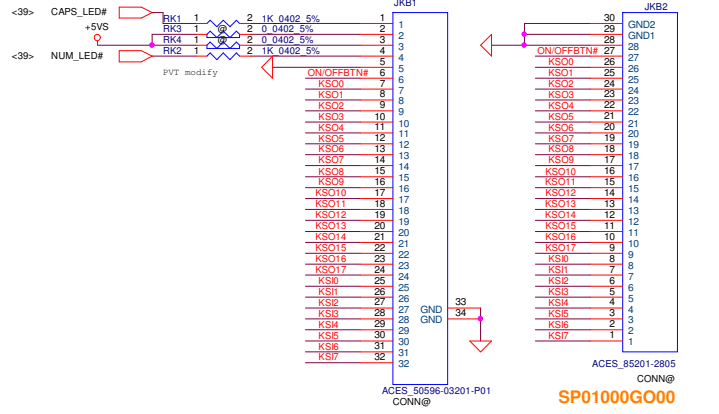


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
				FUN/B & LED/B	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number DHSVF M/B LA-F591PR01
				Date: Thursday, February 22, 2018	Rev 1.0
				Sheet 44	of 67

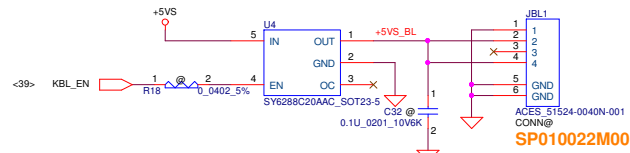
ON/OFF BTN



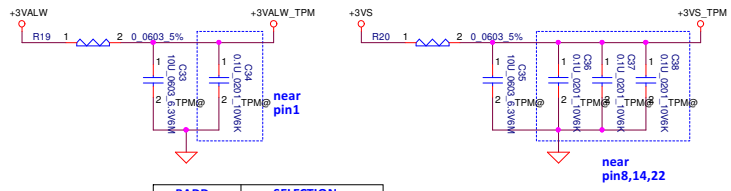
KB Conn.



KB BackLight

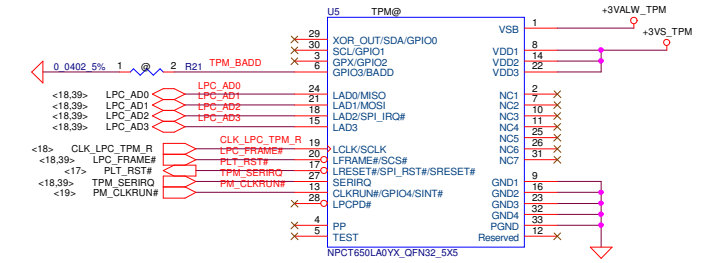
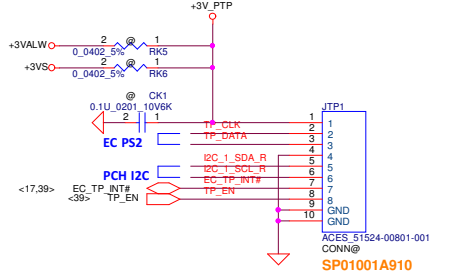
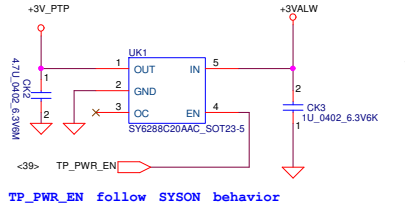


TPM



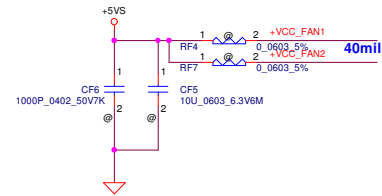
BADD	SELECTION
* 1	Aeh(write), Afh(read)

Touch Pad

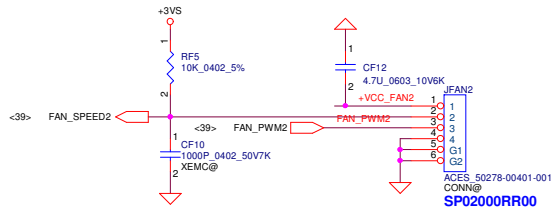
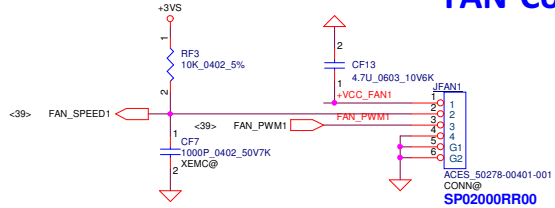


SERIRQ PH 10K to +3VS at PCH side
CLKRUN# PH 10K to +3VS at PCH side
LPCPD# had internal PH

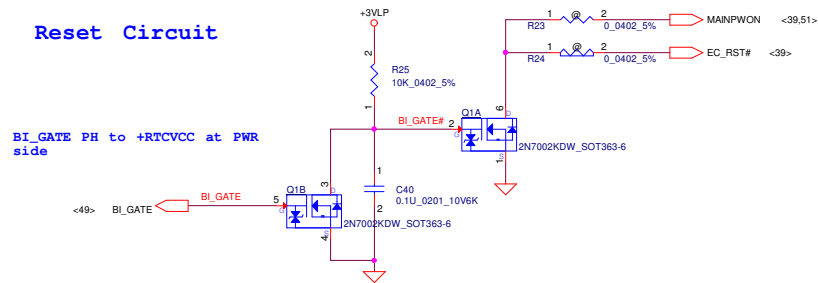




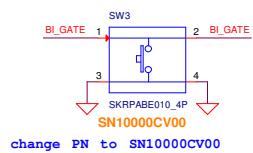
FAN Conn



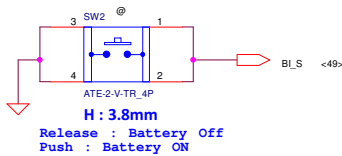
Reset Circuit



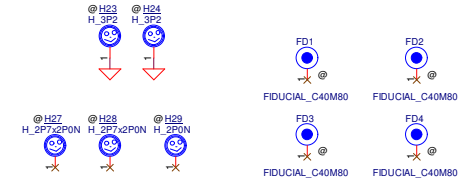
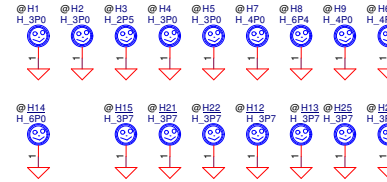
Reset Button



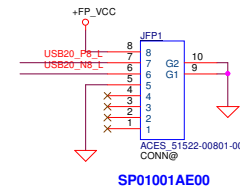
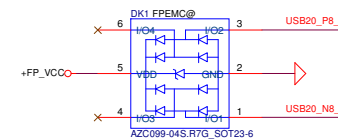
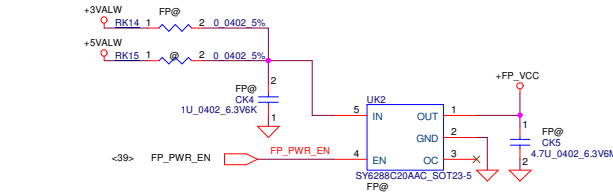
BI SW



Screw Hole



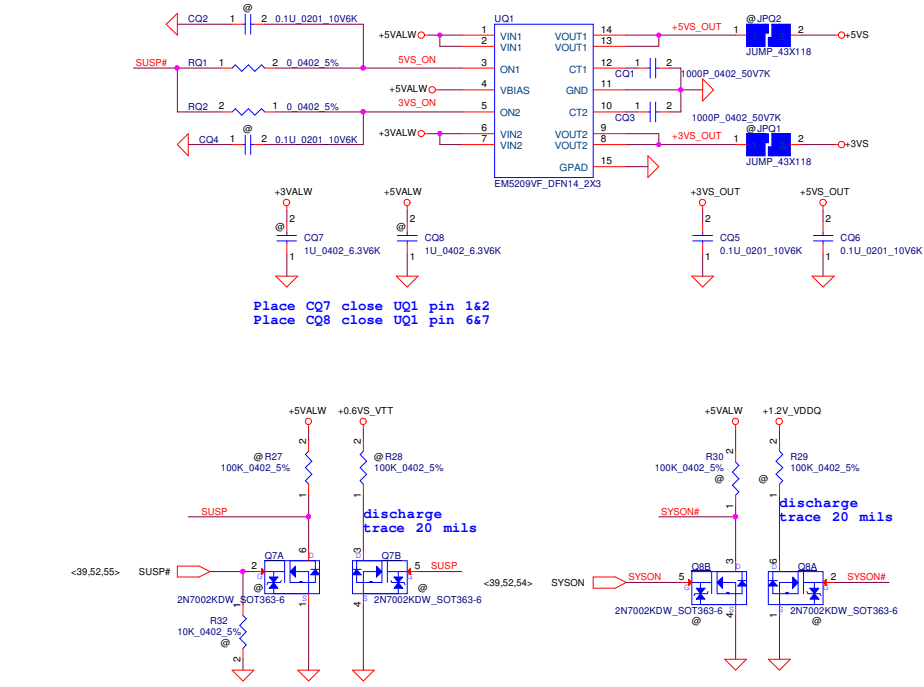
Finger Print



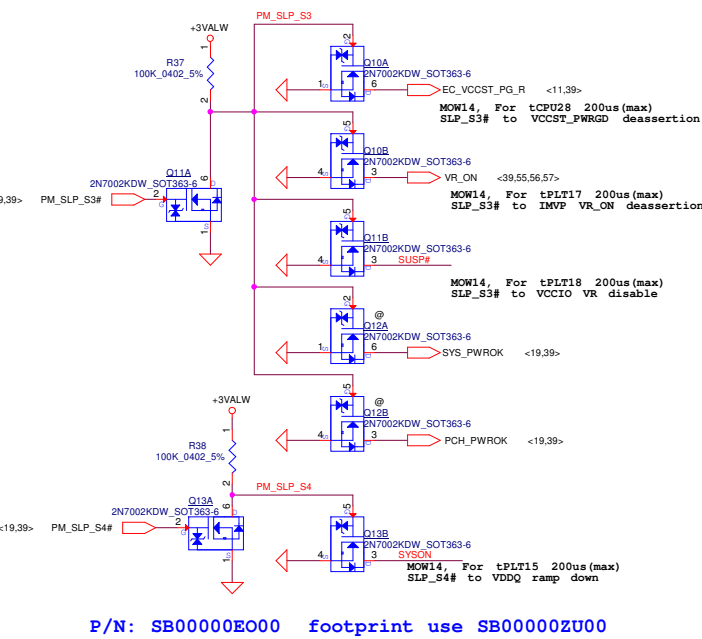
PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	FAN & FP & Screw Hole
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	DH5VF M/B LA-F591PR01
				Date:	Thursday, February 22, 2018
				Sheet	46 of 67
				Rev	1.0

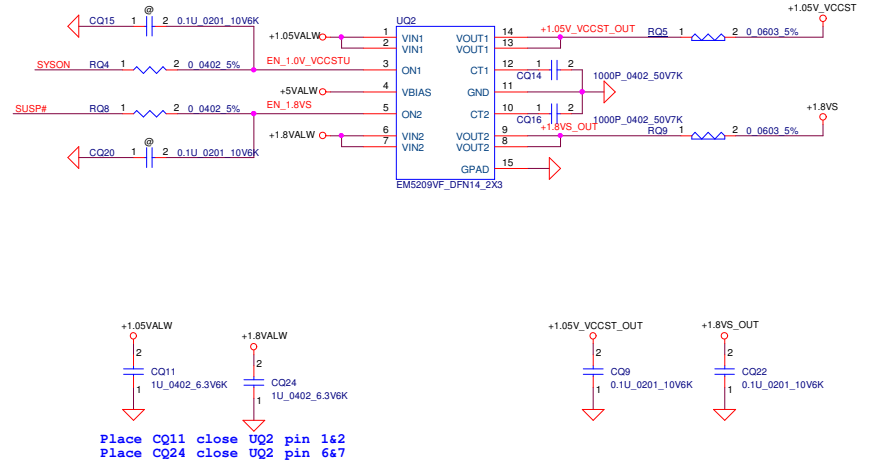
System DC interface



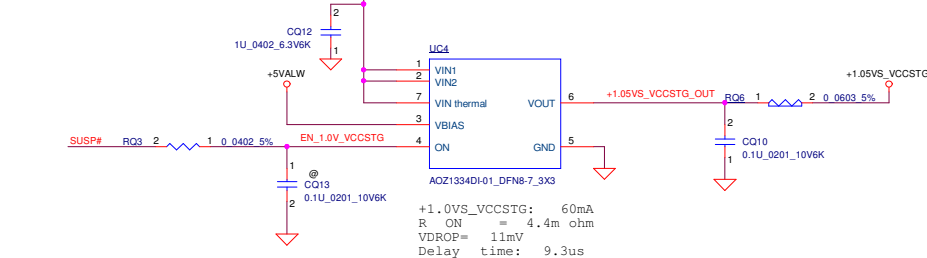
For Power ON/Off Sequence

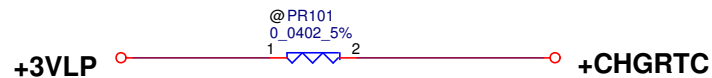
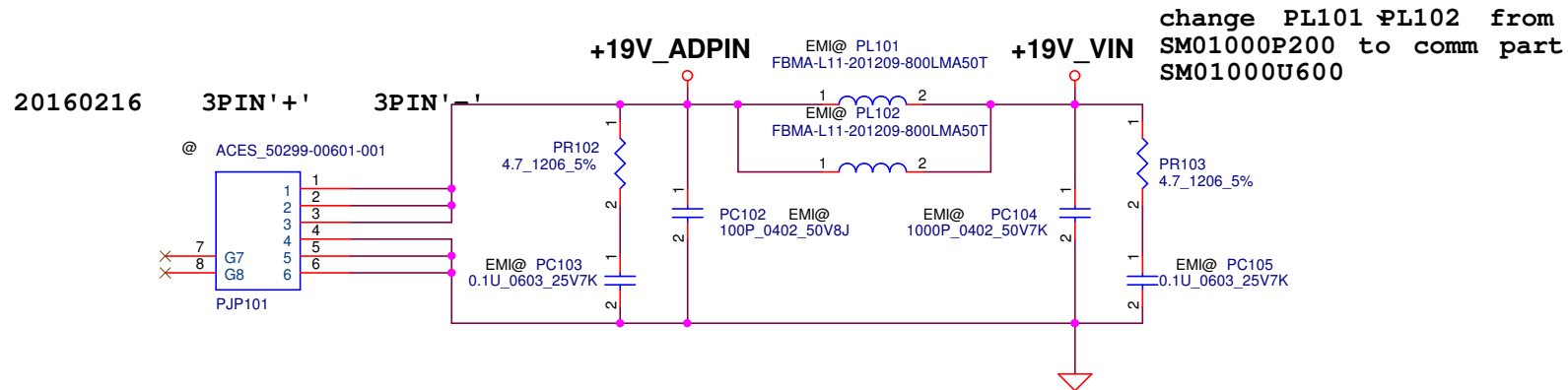


+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS

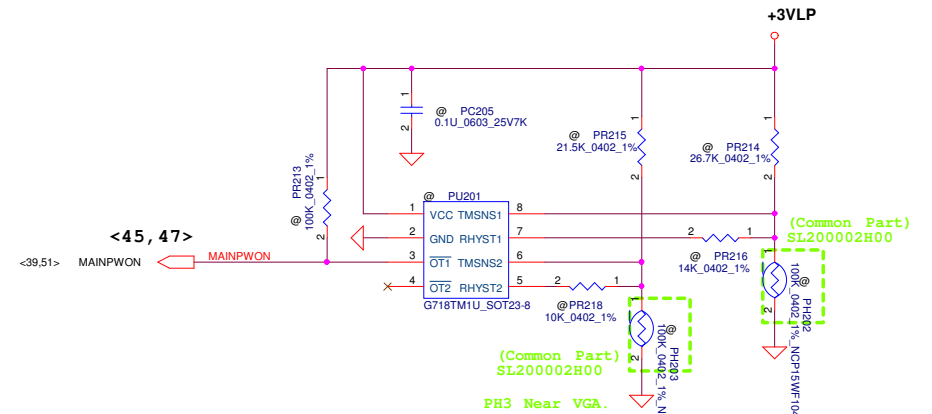
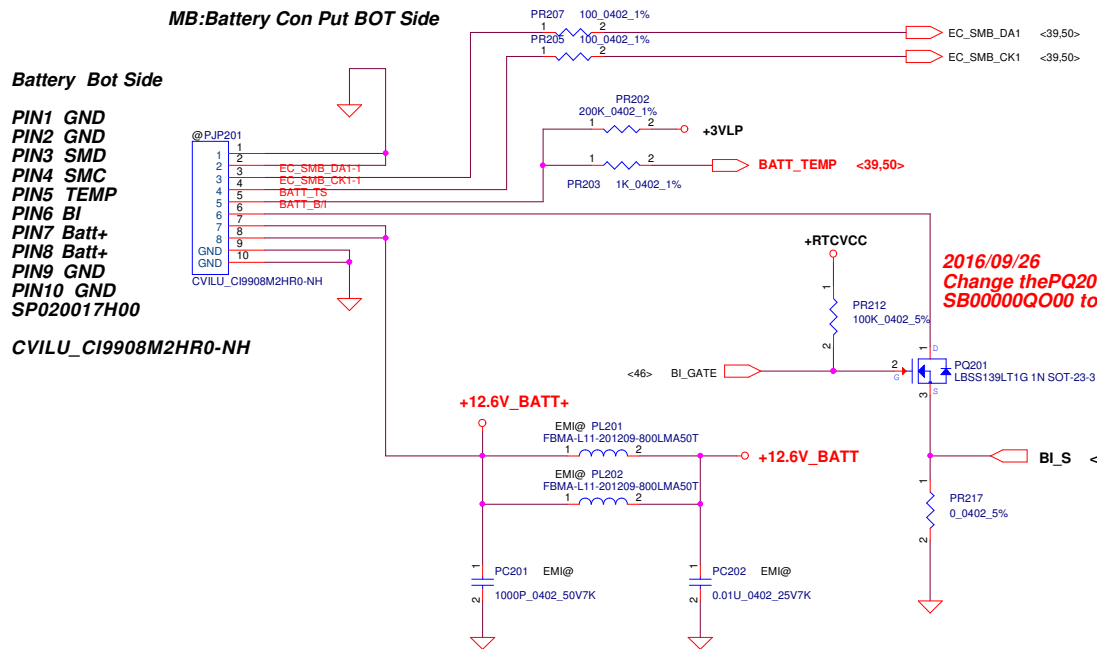


+1.05VALW TO +1.05VS_VCCSTG



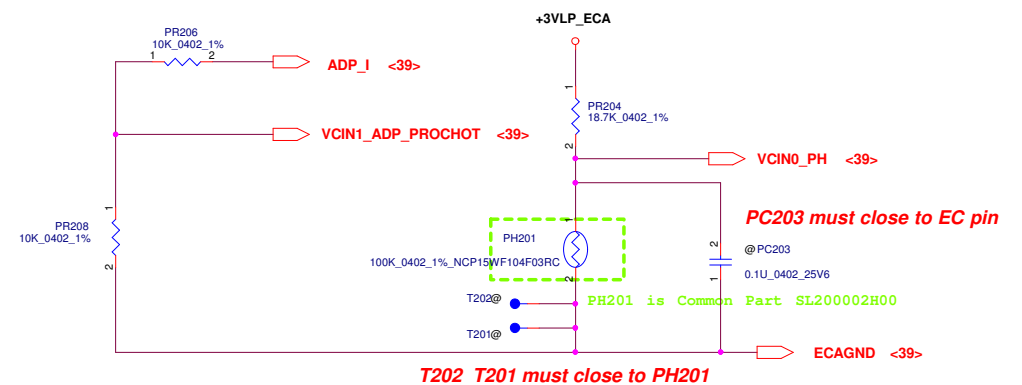


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/07/18	Deciphered Date	2017/06/14	Title	DCIN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number C5MMH M/B LAE911P
				Date:	Thursday, February 22, 2018
				Sheet	48 of 67



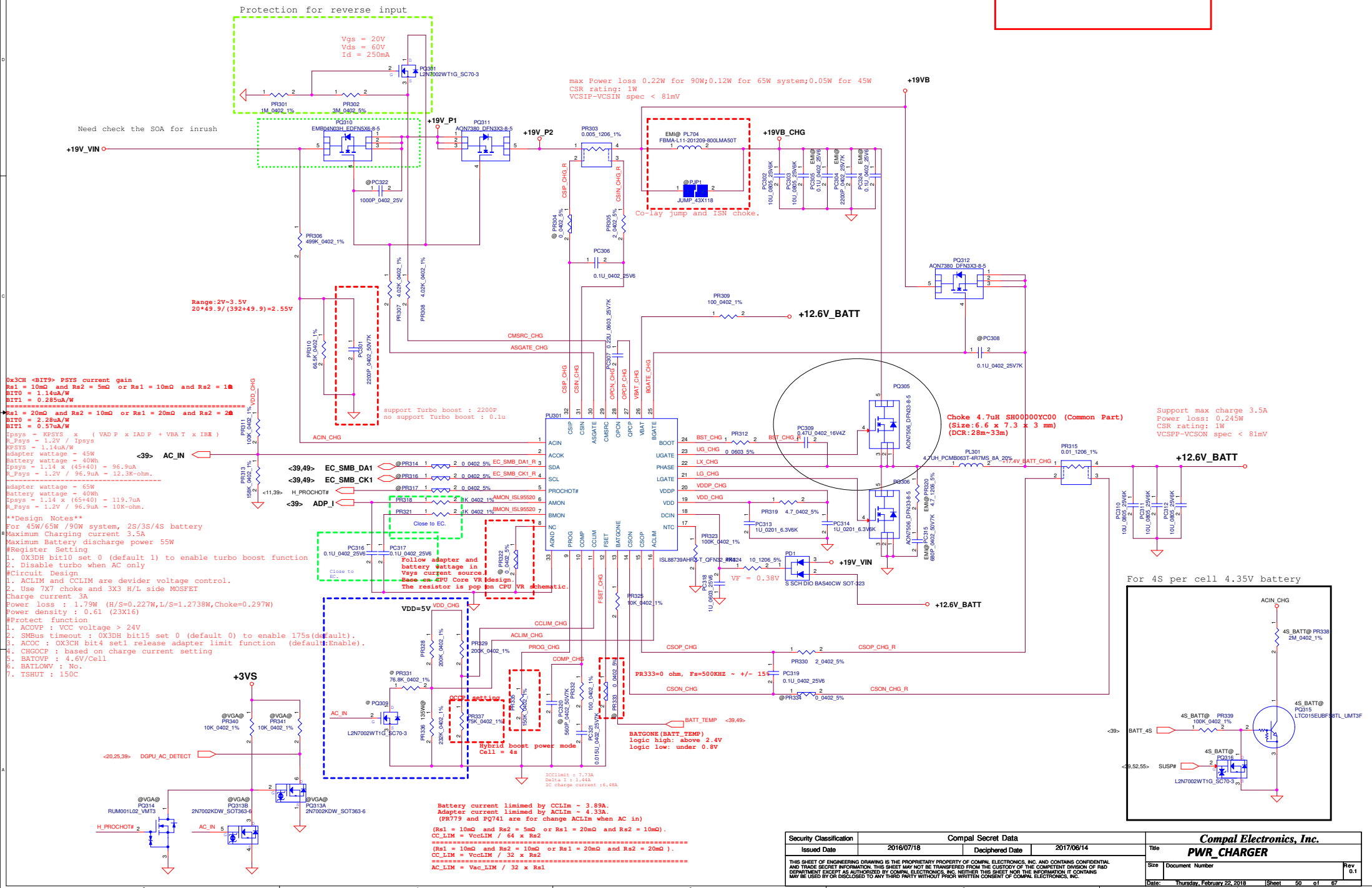
When PR204=16.9K

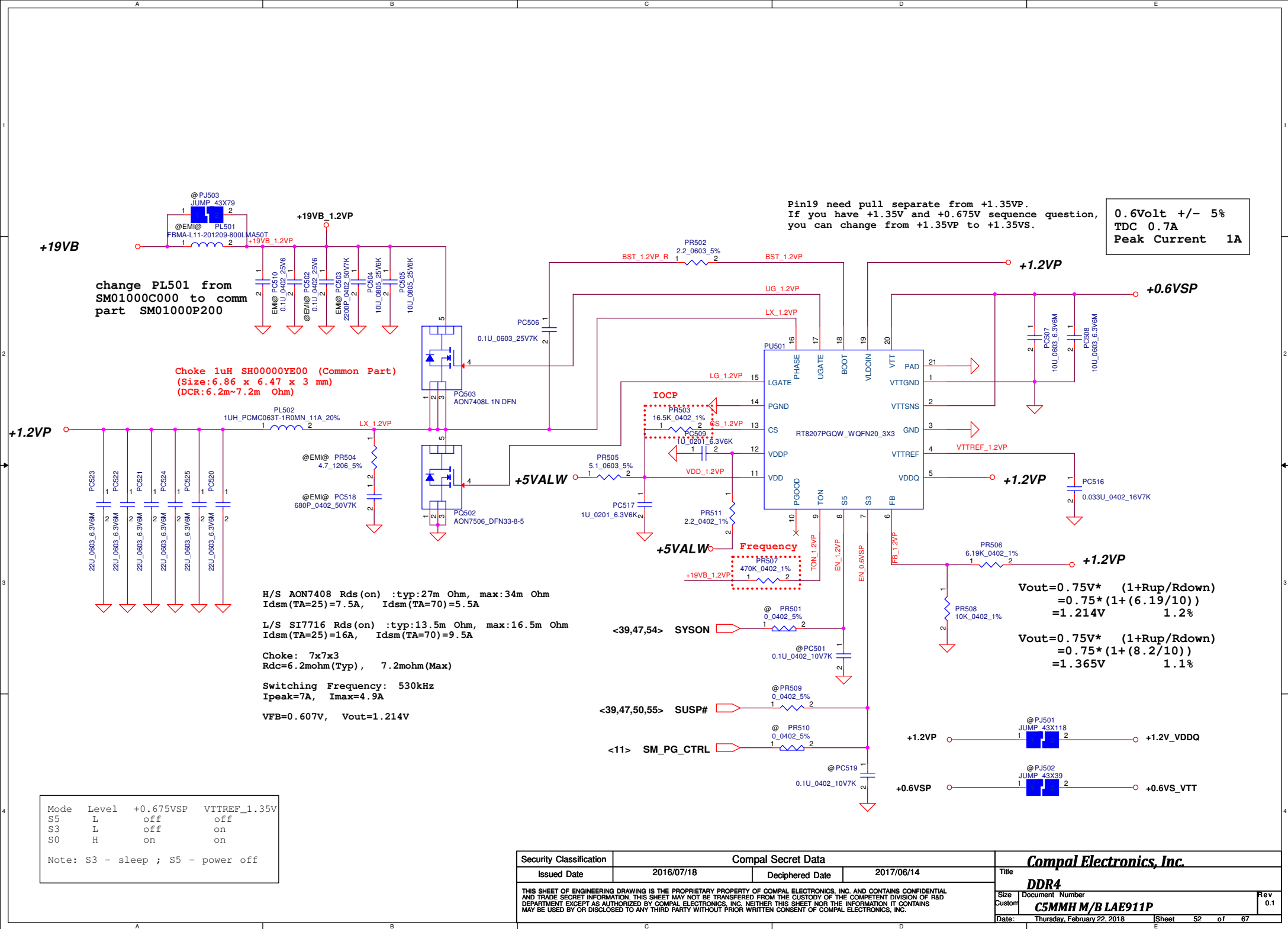
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	89'C, 1V	56'C, 2V
PH202 (ohm)	7.3092K	26.11K



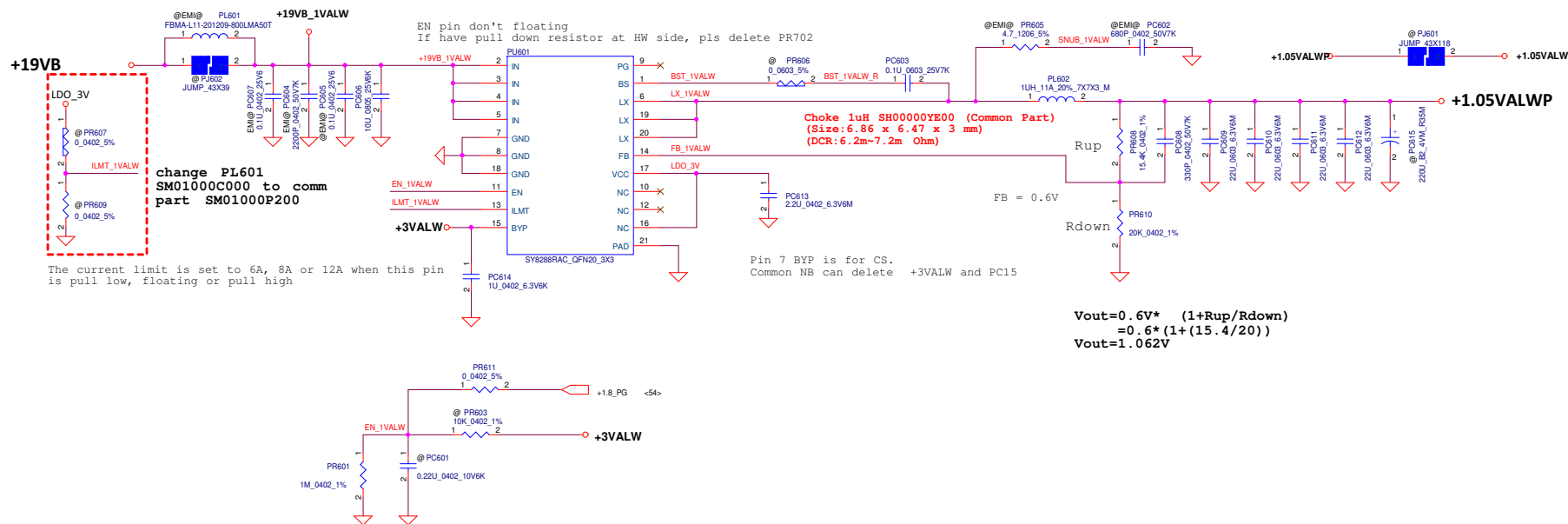
$$ADP_I = 20 * I(\text{adapter}) * 0.01$$

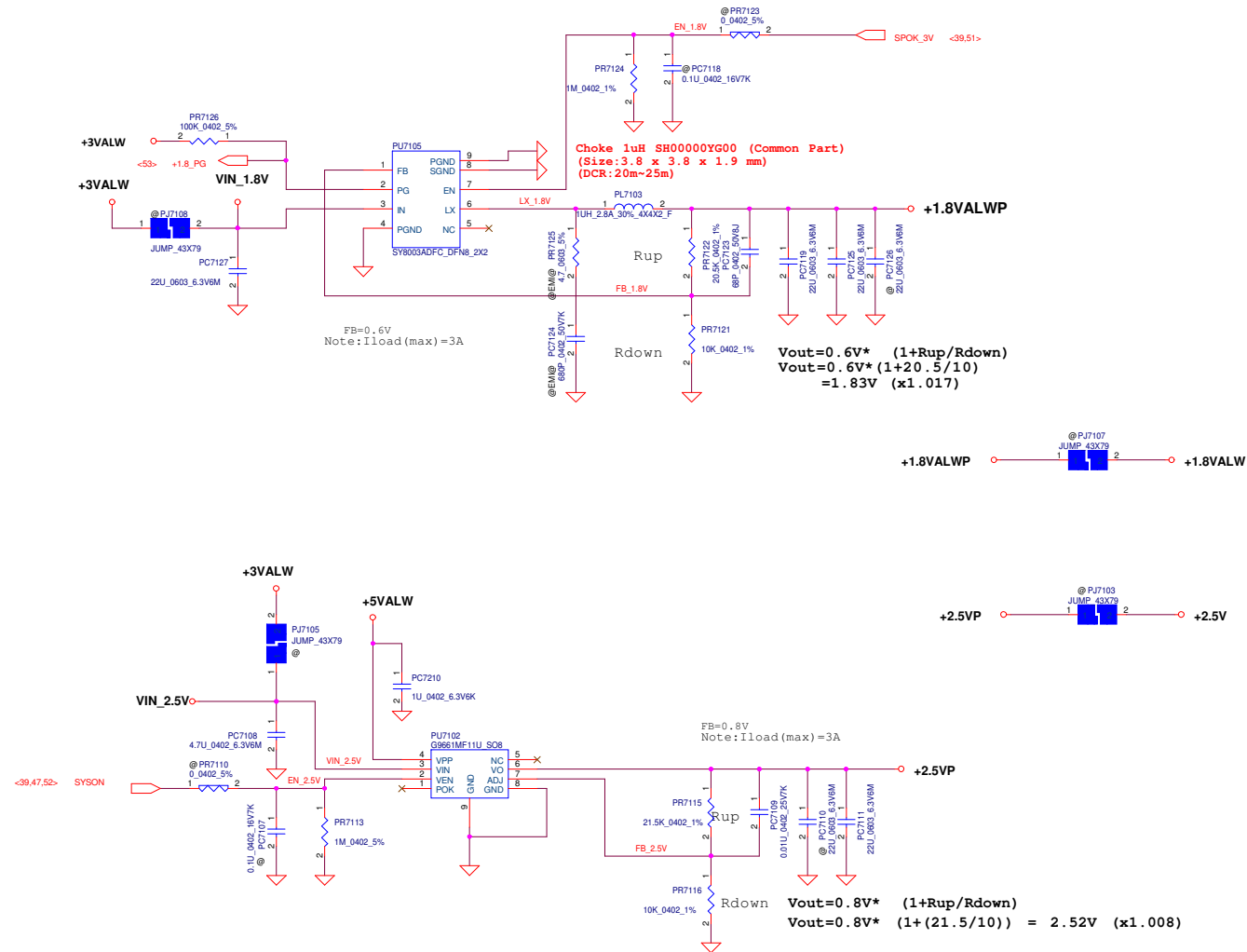
$$I(\text{adapter}) = \text{adapter (W)} * 95\% / 19$$

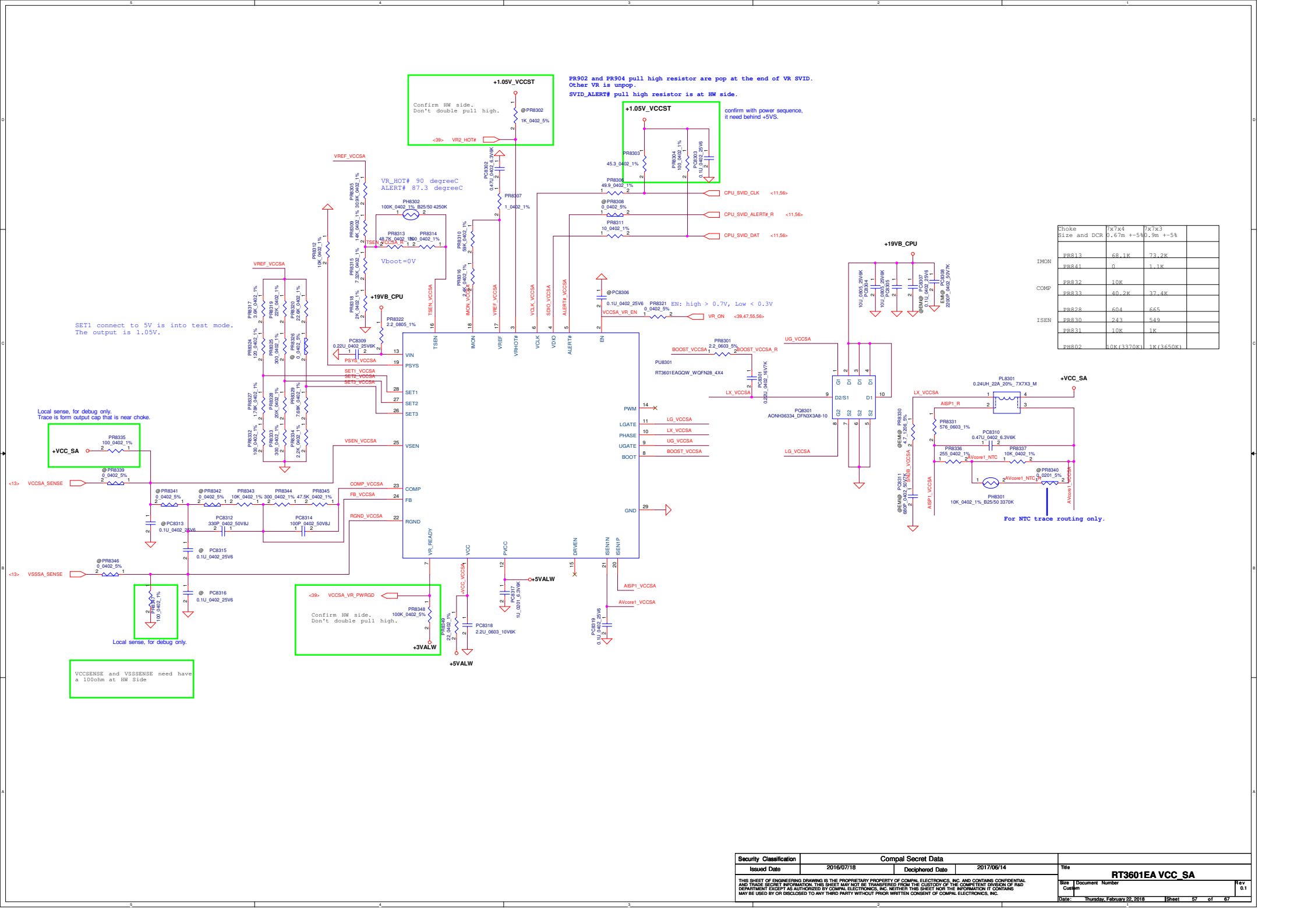




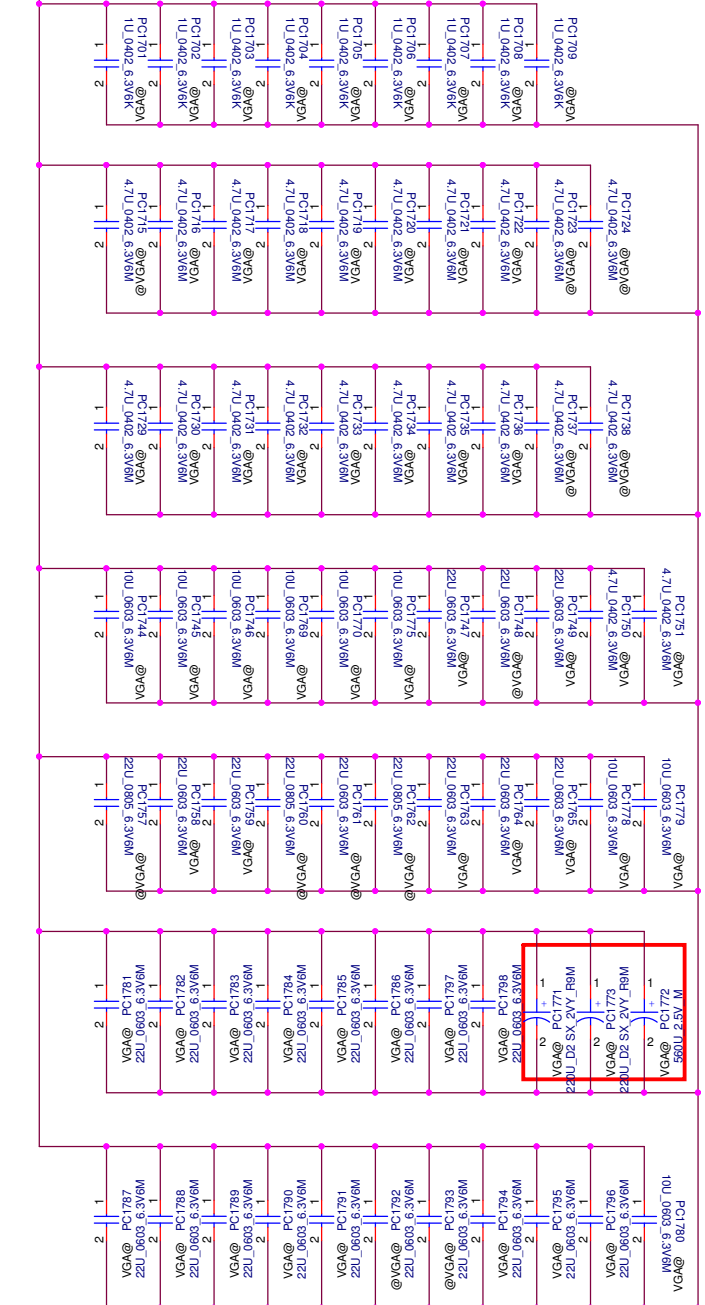
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/07/18	Deciphered Date	2017/06/14	Title	DDR4	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND/OR SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTOMER TO ANY OTHER DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	C5MMH M/B LAE911P	0.1
				Date:	Thursday, February 22, 2018	Sheet 52 of 67





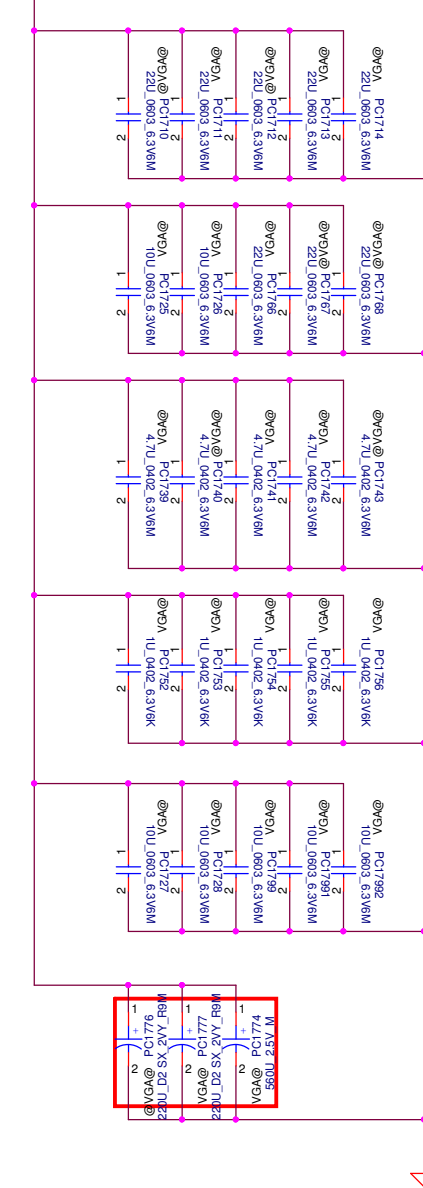


+VGA_CORE



+VGA_CORE
560uF_OS X 2
220uF_D2 X 3(+1@)
22uF_0805 X 0(+3@)
22uF_0603 X 27(+8@)
10uF_0603X 16
4.7uF_0402 X 20(+7@)
1uF_0402 X 14

+VGA_CORE



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Size	
2016/07/18		2017/06/14		Document Number	
2016/07/18		2017/06/14		C5MMH M/B LAE911P	
2016/07/18		2017/06/14		Date: Thursday, February 22, 2018	
2016/07/18		2017/06/14		Sheet 63 of 67	

Version change list (P.I.R. List)

Page 1 of 1 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Solution Change	0.2	50	Change the PQ310 from AON6366E (SB00001D800) to EMB04N03H (SB00001C500). Change the PQ311 P Q812 from AON6366E (SB00001 b800) to AON7380 (SB00001 G M00). Change the PC302 PC303 PC304 PC311 PC312 from 10U_0603_25V (SE00000X200) to 10U_0805_25V (SE00 000Q00). Delete the PC323 10U_0603_25V (SE00000X200).	10/13	A2
02	Design Update	Solution Change	0.2	53	Change the PR603 (10K_0402_1%, SD034100280) from pop to un-pop.	10/13	A2
03	Design Update	Solution Change	0.2	54	Change the PR7126 (100K_0402_5%, SD028100380) from un-pop to pop. Change the PR7126.2 net from +3VS to +3VALW.	10/13	A2
04	Design Update	Solution Change	0.2	63	Change the PC1748 PC1761 PC1770 PC1772 PC1767 PC1768 (22U_0603_6.3V, SE0 0000M000) from pop to un-pop.	10/13	A2
05	Design Update	Down size for SNB MLCC	0.2	50、59、62	Change the PC315 PC1308 PC152 PC152 PC152 from 680P_50V_K_X7R_0603 (SE025681K80) to 680P_50V_K_X7R_0402 (SE074681K80).	10/13	A2
06	Design Update	Solution Change	0.2	59	Change the PQ1302 from 2N7002KW (SB000009Q80) to L2N7002WT1G (SB000005T00).	10/13	A2
07	Design Update	Down size for MLCC	0.2	59	Change the PC1307 from 1U_6.3V_M_X5R_0603 (SE107105M80) to 1U_6.3V_K_X5R_0402 (SE000000K80).	10/13	A2
08	Design Update	Down size for EMI MLCC	0.2	48	Change the PC102 from 100P_50V_J_NPO_0603 (SE024101J80) to 100P_50V_J_NPO_0402 (SE071101J80). Change the PC104 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80).	10/13	A2
09	Design Update	Down size for MLCC	0.2	63	Change the PC1747 PC1759 PC1779 PC1788 PC1764 PC1766 P from 22U_6.3V_M_X5R_0805 (SE000000I10) to 22U_6.3V_M_X5R_0603 (SE000000M000).	10/13	A2
10	Design Update	Solution Change	0.2	56	Change the PH8103 PH8104 from 150K_5%_0402_B25/50_4500K (SL200002K00) to 220K_5%_0402_B25/50_4700K (SL200002I00). Change the PR8109 PR8110 from 8.87K_0402_1% (SD034887180) to 8.66K_0402_1% (SD034866180). Change the PR8118 PR8119 from 931K_0402_1% (SD034931280) to 57.6K_0402_1% (SD034576280).	10/23	A2
11	雷雕區	Down size for Jump	0.2	53	Change the PJ602 from 43X79 to 43X39.	10/23	A2
12	Design Update	Solution Change	0.2	56、57	Change the PC8113 PC8124 PC8140 PC859 PC818 from 0.47U_16V_Z_Y5V_0402 (SE000002F80) to 0.47U_6.3V_K_X5R_0402 (SE124474K80). Change the PC8310 from 0.47U_25V_K_X5R_0402 (SE00000WA00) to 0.47U_6.3V_K_X5R_0402 (SE124474K80).	10/25	A2
13	Design Update	Solution Change	0.2	58	Add the location PC9164 PC9165 PC9166 and pop. 22U_6.3V_M_X5R_0603 (SE0000 0M00)	10/26	A2
14	Design Update	CPU transient test result	0.2	56、57、58	Change the PR8114 from 6.81K_0402_1% (SD034681180) to 5.76K_0402_1% (SD034576180). Change the PR8113 from 2.49K_0402_1% (SD034249180) to 1.8K_0402_1% (SD00000R580). Change the PR8117 from 560K_0402_1% (SD034560380) to 442K_0402_1% (SD034442300). Change the PR8116 from 510K_0402_1% (SD00000RK80) to 402K_0402_1% (SD034402380). Change the PR8141 from 100_0402_1% (SD034100080) to 8.2K_0402_1% (SD000004100). Change the PR8149 from 1.05K_0402_1% (SD00000J480) to 3.16K_0402_1% (SD000006580). Change the PR8176 from 20K_0402_1% (SD034200280) to 16.9K_0402_1% (SD034169280). Change the PR8310 from 63.4K_0402_1% (SD03463K280) to 59K_0402_1% (SD034590280). Change the PR8319 from 24.9K_0402_1% (SD034249280) to 22K_0402_1% (SD034220280). Change the PR8325 from 0_0402_5% (SD028000080) to 300_0402_1% (SD034300080). Change the PR8328 from 22K_0402_1% (SD034220280) to 20K_0402_1% (SD034200280). Change the PR8333 from 680_0402_1% (SD034680080) to 300_0402_1% (SD034300080). Change the PC8312 from 270P_0402_50V7K (SE074271K80) to 330P_0402_50V8J (SE000006I80). Change the PR8331 from 470_0603_1% (SD014470080) to 576_0603_1% (SD014576080). Change the PR8336 from 42.2_0402_1% (SD00000ZNO0) to 255_0402_1% (SD034255080). Change the PR8134 from 121K_0402_1% (SD034121380) to 13.3K_0402_1% (SD034133280). Change the PR8138 from 49.9K_0402_1% (SD034499280) to 26.7K_0402_1% (SD034267280). Change the PR8147 from 3.32K_0402_1% (SD034332180) to 768_0402_1% (SD00000TT80). Change the PC9110 PC9108 from 22U_0603_6.3V6 M (SE00000 M000) to un-pop Change the PC9112 PC9113 from un-pop to 22U_0603_6.3V6 M (SE00000 M000) Change the PC8126 from 330P_0402_25V8J (SE00000FD80) to 330P_0402_50V8J (SE000006I80). Change the PR8173 from 0_0603_5% (SD013000080) to 10_0603_1% (SD014100A80). Change the PC8137 from 330P_0402_25V8J (SE00000FD80) to 270P_0402_50V7K (SE074271K80). Change the PC9159 PC9160 from 22U_0603_6.3V6 M (SE00000 M000) to un-pop Change the PC9057 PC9058 from un-pop to 22U_0603_6.3V6 M (SE00000 M000)	10/27	A2
15	Design Update	Power sequence	0.2	59、60	Change the PR1303 from 10K_0402_1% (SD034100280) to 1K_0402_1% (SD034100180). Change the PR1401 from 10K_0402_5% (SD028100280) to 4.7K_0402_5% (SD028470180).	11/02	A2
16	Design Update	Solution Change	0.2	61	Change the PU1201 from UP9511P (SA00009SW00) to UP9511Q (SA00000BK300). Change the PR1243 PR1247 from 10K_0402_5% (SD028100280) to 100K_0402_5% (SD028100380).	11/08	A2
17	Design Update	Solution Change	0.2	52、56、57	Change the PC8317 PC509 PC517 from 1U_0402_10VK (SE0000 0Q10) to 1U_0201_6.3V6K (SE00000YB00). Change the PC8112 PC8115 PC812 PC819 PC857 PC8161 from 1U_0402_25V6K (SE000010V00) to 1U_0201_6.3V6K (SE00000800).	11/08	A2
18	Design Update	Solution Change	0.2	50、56	Change the PR340 P Q814 P Q312 PC33B PC327 PC307 PC308 from pop to un-pop. Change the PR326 from un-pop to 0_0603_5% (SD013000080). Change the PR310 from 51.1K_0402_1% (SD034511280) to 52.3K_0402_1% (SD034523280). Change the PC8147 from 10U_0805_25V_X5R (SE00000QK00) to un-pop	11/14	A2

Security Classification

Compal Secret Data

Issued Date

2016/01/29

Deciphered Date

2017/06/14

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title

PIR

Size Document Number

DH53F M/B LA-E951P

Rev

0.1

Date: Thursday, February 22, 2018

Sheet 64 of 67

Version change list (P.I.R. List)					Page 2 of 2 for PWR			
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase	
19	Design Update	Solution Change	1.0	50	Change the PC313 PC314 from 1 U_16V_X5R_0402 SE000000U00 to 1 U_6 3V_X5R_0201 (SE00000YB00).	12/15	C	
20	Design Update	Solution Change	1.0	50、55 56、57	Change the PR304 PR314 PR36、PR22、PR34、PR111、R8120 PR8128 PR8139 PR812、PR813、PR853、PR81 54、PR8155 PR8165 PR810、PR875、PR890、PR129、R8163 PR8184 PR8198 PR820、PR808、PR826、PR8 39、PR8341 PR8342 PR836、PR87、PR 333 from 0_0402_5%(SD028000080) to R-short	12/15	C	
21	Design Update	Solution Change	1.0	50	Change the PC305 PC324 from 01 U_0402_25V7K(SE00000 W210) to 01 U_0402_25V6(SE00000G880).	12/18	C	
22	Design Update	Solution Change	1.0	56	Change the PC8101 PC8122 PC815、PC850、PC8158 from 0.1U_0603_50V7K(SE025104K80) to 0.1U 25V K X7R 0603 (SE042104K80).	12/18	C	
23	Design Update	SW2 un-pop	1.0	49	Change the PR217 from un-pop to 0_0402_5%(SD028000080).	12/18	C	
24	Design Update	Solution Change	1.0	50	Change the PR326 PR7202 from 0_0603_5% SD013000080) to R-short	12/18	C	
25	Design Update	Solution Change	1.0	56	Add PC8116 PC8118 33U_01_25V M_R6 M(SG A0000 A400), and un-pop	12/19	C	
26	Design Update	4S_BATT	1.0	50	Delete location PR326 PR327 PC307、PC8 Add location PR338->2M_0402_1%(SD034200480) PR339->100K_0402_1%(SD034100380) Add location PQ315->LTC015EUBFS8TL(SB000011K00) P Q816->2N7002K WI N SOT323-3 (SB00000ST00)	12/20	C	
27	Design Update	Solution Change	1.0	50	Change the PC309 from 0.22U_0603_25V(SE0000005Z80) to 0.47U_0402_16V(SE0000002F80).	12/21	C	
28	Design Update	ACIN_CHG	1.0	50	Change the PR306 from 392K_0402_1%(SD034392380) to 499K_0402_1%(SD034499380). Change the PR310 from 52.3K_0402_1%(SD034523280) to 66.5K_0402_1%(SD034665280).	12/25	C	
29	Design Update	Power sequence	1.0	60	Change the PR1406 from 10K_0402_1%(SD034100280) to 0_0402_5%(SD028000080).	12/27	C	
30	Design Update	3valw interfere	1.0	55、59	Change the Jump PJ7202 PJ1301 from mshort to open Change the bead PL7201 PL1301 from un-pop to pop 0805_5A(S M01000U600). Change the PR7203 from un-pop to pop 4.7_1206_5%(SD001470B80) Change the PC7203 from un-pop to pop 680pF_0402_50V (SE074681K80)	01/10	C	
31	Design Update	Solution Change	1.A	55	Change the PR7202 from R-short to 0_0603_5%(SD013000080).	01/12	C	

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	29	Design Update	9/27	power source optimization	DGPU1.8V power source change to 1.8VALW	A2	0.2
2	39	Design Update	9/27	version upgrade	Change board ID to DVT (V15_ID1/VX15_ID11)	A2	0.2
3	37	Design Update	10/17	CNVI power request	Add RM44 for +3VALW to +3VS_WLAN	A2	0.2
4		Design Update	10/19	0 ohm part count reduce	RH186/RH47/RH103/RH105/RH97/RH98/RH99/RH100/ RD3/RD6/RD2/RD15/RD13/RD17/RM22/RM23/RM24/ RM25/RM26/RM27/RM28/RM29/RM30/RM31/RM32/ RM33/RM34/RM35/RM38/RM39/RM40/RS1/RS8/RS16/ R19/R20/RQ5/RQ9/RQ6	A2	0.2
5	41,42	Design Update	10/19	USB common voltage footprint update	LS1/LS10 change footprint to "MURAT_DLM0NSN900HY2D_4P"	A2	0.2
6		Design Update	10/24	for cost, change 10uF_0402 to 0603	CV75, Cv83, CV86, Cc88, CV87, Cv83, Cv73, Cv82,Cv108, Cv119, Cv118, Cv110, Cv120, Cv121, Cv114, Cv115 , CC75, Cc73, Cc80, CC74,CC76, CC78, CC79, CX1 CX3, CA6, CA8, CA9, CA16, CA17, CC71, CC72, CC81, CC89, CC90,	A2	0.2
7	44	Design Update	10/25	USB CMC move to M/B	add L11/ L12 for USB2.0 CMC	A2	0.2
8	39	Design Update	10/26	CNVI device detect issue	add PU 100K RB78 for CNVI card detect reserved RB79 PD 0ohm for CNVI card detect EC add PIN89 GPIO50 as CNVI_DET# add PIN 19 CNVI_DET#	A2	0.2
9	38	Design Update	10/26	for reserve 4 dmic	Change JDMIC1 to 4pin : SP02000TI00	A2	0.2
10	43	Design Update	11/02	SATA HDD redriver EQ tuning	UNPOP RO17 for redriver EQ	A2	0.2
11	25	Design Update	11/02	NV vga sequence tuning	change RV105 to 8.2K (vga_core_en) RV12 change to 100k_1% (I.35VSDGPU_PWR_EN) RV113 change to 4.7k_5% PR1303 change to 1k PR1401 change to 4.7k	A2	0.2
12	43	Design Update	11/06	co-lay no HDD re-driver circuit	add CO14/CO16~18/RO21~24 for no re-driver.	A2	0.2
13	45	Design Update	11/13	for factory request, don't include SW1 in bom	unpop SW1 and control by SMT memo	A2	0.2
14	40	Design Update	11/13	replace level shift by 0 ohm on Type-C circuit	unpop QS1/RS107/RS108 POP RS114/RS115	A2	0.2
15		Design Update	11/13	fine tune crystal frequency	24Mhz Keep 33 18 /1M 25Mhz Keep 10 18 /330 27Mhz CV1 change to 15PF (15 12 /0) 32.768Khz change CH7/CH8 to 10PF (10 10 /10M)	A2	0.2
16		Design Update	12/14	0 OHM change to R-short	change RC17/RH5/RH6/RH94/RH96/RV125/RM2/RB19/RB76/RO4 /RS114/RS115 to R-short	PVT	1.0
17	18	Design Update	12/14	peci issue, can't get system temperature	UNPOP RH41	PVT	1.0
18	46	Design Update	12/14		unpop SW2(BI SW)	PVT	1.0
19	39	Design Update	12/16		change board ID to ver1.0 (V series 15k/ vx series 200k)	PVT	1.0
20	40	Design Update	12/18	change typeC VCONN sol to G527	add RS116 on VBUS_EN_179 change US2 to SA00006Y700, add RS156/RS155/CS101/CS124	PVT	1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	PIR-HW1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev 1.0
				Date:	Thursday, February 22, 2018	Sheet 66 of 67

Security Classification		Compal Secret Data		Compal Electronics, Inc. PIR-HW1	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number DH5VF M/B LA-F591PR01
				Date:	Thursday, February 22, 2018
				Sheet	67 of 67
				Rev	1.0